Technical Memorandum
LOW RESOLUTION RADAR DIGITAL INTERFACE

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TECHNICAL REPORT 2374-14

May 1973

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National Aeronautics and Space Administration
Office of Grants and Research Contracts
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ABSTRACT

This technical report is a working document which describes the design and operation of a low resolution radar data recording system for precipitation measurements. This system records a full azimuth scan on seven track magnetic tapes every five minutes. It is designed to operate on a continuous basis with operator intervention required only for changing tape reels and calibration.

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I. LOW RESOLUTION RADAR SYSTEM DESCRIPTION

A. Introduction

The Low Resolution Radar System (LO-RES system) is a fully automated system designed for 24 hour/day, unmanned data acquisition. This system utilizes a conventional 9 GHz commercial marine pulse radar and 0.7 m parabolic antenna. The antenna rotates continuously in azimuth with a fixed elevation angle. Every five minutes the radar video signal is sampled and digitally integrated over one complete antenna rotation. If the integrated backscatter is larger than a preset threshold level, the successive scan is digitized and recorded on magnetic tape. The date, time, azimuth angles, and transmitted power levels are also recorded on this magnetic tape. The radar data may also be displayed on a conventional 360° PPI display with a maximum range of 100 Km. This system provides the capability for gathering statistical data concerning size, intensity, shape, orientation, and movement of thunderstorm cells continuously over long periods of time.

This capability was developed for the measurement of the temporal and spatial characteristics of precipitation in conjunction with millimeter wavelength propagation studies utilizing the Advanced Technology Satellites. The precipitation characteristics derived from these measurements could also be of direct benefit in such diverse areas as: the atmospheric sciences, meteorology, water resources, flood control and warning, severe storm warning, agricultural crop studies, and urban and regional planning.

This technical report is a working document which describes the design and operation of the low resolution radar data recording system. This system records a full azimuth scan on seven track digital magnetic tape every five minutes. It is designed to operate on a continuous basis with operator intervention required only for changing tape reels and calibration. As the system is operated and the data analyzed, changes will be made in the design to improve the operation. Thus, this document is expected to be continuously updated to reflect these changes. The computer software is also described.

B. System Description

The low resolution radar system has three major components. The first of these is a Kelvin Hughes Marine radar. The characteristics of this radar are summarized in Table I. The second component is an SDS 910 computer which is described in Table II. The third component is a digital interface which was designed and constructed at the ElectroScience Laboratory. The interface accepts video data from the

TABLE I
KELVIN HUGHES MARINE RADAR MODEL

Frequency	9.458	GHz
Repetition Rate	800	Hz
Pulse Width	.75	μs
Peak Power	18.6	kW
Antenna Beamwidth	1.2°	Azimuth x 25° elevation at 3 dB points
Scan Rate	24	rpm

TABLE II
SDS 910 COMPUTER

Word Size	24 bits
Core Size	2048 words
I/O Capabilities	24 bit parallel input and output
	6 bit character buffer
Interrupts	4 priority level
Cycle Time	8 μs, most instructions 2 to 3 cycles
Peripherals	Paper tape reader
	Tape drive; 7 track, 200 bpi

The characteristics and timing parameters used to specify the operation of the interface will be discussed first. Next the overall operation of the interface will be explained. This will be followed by a discussion of the individual circuits in the interface. Finally the data format and processing techniques will be described.

C. Interface Characteristics

The Kelvin Hughes radar has an effective range of seventy-two miles. For the purposes of data collection a zero to fifty mile range was considered. The antenna azimuth beamwidth at ranges beyond fifty miles was considered to be too wide to provide useful data. A convenient number of range bins, based on component availability and storage capability of the computer and magnetic tape reel, was found to be one hundred. Using the criterion that the fiftieth range bin should be approximately square, the range bin depth was found to be approximately 0.7 km. This corresponds to an A/D sampling period of slightly more than 5 μs. A sampling period of 6 μs was chosen. Thus, a range bin is 0.9 km deep. Since only gross radar backscatter data were sought three bits were used in the A/D conversion. An

eight bit A/D converter was used in the hardware so that if three bits were found to be insufficient the data could be extended to a maximum of eight bits. This would however involve some redesign of the interface circuitry to accommodate the larger video data word.

A target detection scheme was desired so that the recording of data would occur only when a storm was present in the zero to fifty mile range. So that the entry of a storm into the data region could be recorded the full seventy-two mile range capability was used for target detection. The scheme used involves digitally integrating the entire video return from one radar scan. An integration in range for each antenna look angle and an integration of each range sum for all look angles are performed. The result is then compared to a threshold level to determine if a target is present. Because there are two integrations, two levels of target detection are possible. After one hundred range bins are integrated for a look angle a comparison can be made to set a range target flag. After a scan is completed a comparison can be made to determine if a target is present in the scan area. The interface has provisions for both target flags to control the transmission of data to the computer. However, the current version of the SDS 910 software requires that a full scan be recorded on magnetic tape so only the azimuth integration target flag is used. The range integration flag currently remains set.

Along with the Kelvin Hughes radar, a digital clock and power monitor are connected to the interface. Thus, the recorded data has the date and time of the scan, the azimuth look angle, the average power of the radar at the time of the look angle and one hundred samples of the radar video. For each look angle, fifteen 24 bit words are required to transfer this data to the computer. These are written in 855 word records on seven track digital magnetic tape. To limit the amount of data recorded to a reasonable level the interface operates only once every five minutes. Thus, a 2400 foot reel of magnetic tape can hold the data for approximately twenty-five hours of continuous recording. The various signals transferred from the Kelvin Hughes radar to the interface are described in the following section. A power divider was inserted at the preamplifier output for the signal return input of the interface. A logarithimic amplifier with a nominal 80 dB dynamic range was used to provide the video signal. The scanning system in the Kelvin Hughes radar develops a -20V pulse to provide a heading line on the PPI display. This pulse occurs once each antenna revolution and is used by the interface to signal the start of an azimuth scan. The pulse occurs each time the antenna is pointed due North. Also used by the scanning circuitry is a 36 Hz, 85V p-p 2 phase signal which drives the PPI display deflection yoke. The zero crossings of each phase, when combined, occur at one degree increments in azimuth as the antenna scans. These signals are used by the interface to determine the antenna pointing angle. The power monitor

mentioned earlier is coupled to the antenna transmission line and measures the actual transmitted power.

The SDS 910 computer also uses several signals to control the transfer of data from the interface to the computer. To signal that the interface is ready with data the priority interrupts are used. The first level has been reserved for implementation of an abort interrupt. Levels two, three and four are used by the interface to signal the type of data to be transferred to the computer. Because of limitations in the computer, the intended use of these interrupts for controlling an interfaced magnetic tape-interface operation could not be implemented. Although all levels are currently used, two levels could be used for other purposes without impairing the operation of the interface. This is discussed in more detail in the description of the interrupt control module.

The actual data transfer from the interface to the computer is done through the parallel input buffer of the computer. A ready signal from the interface initiates the data transfer by causing a parallel input instruction, PIN, to be executed by the computer. A finished signal from the buffer indicates when the imput process is complete. Although there are other signals present, only these two are used by the interface for the parallel input operation.

II. INTERFACE CONSTRUCTION AND OPERATION

A. Introduction

The three basic components of the low resolution radar system have been described. The Kelvin Hughes radar and SDS 910 computer characteristics have been explained. The signals from these units which are used by the interface have been described. In this section the construction and operation of the interface will be discussed and the circuit and timing diagrams will be presented. General comments about the construction techniques used will also be discussed. Specific construction details are presented in Appendix B.

B. Construction Comments

The digital interface was fabricated using high density dual-in-line packaging panels for the logic circuits. These panels are sometimes referred to as wire wrap boards. Each panel is a glass epoxy circuit board with individual terminals for each integrated circuit package pin. The terminals have half inch tails to which wires are wrapped to make a connection. Each terminal can have three wraps using conventional wire wrap techniques. The terminals are arranged in the conventional sixteen pin dual-in-line pattern, TO-116.

Each panel has 60 socket patterns arranged in two groups. At the head of each group are two groups of header pins used for external connections.

The wire wrap type of construction was chosen for its flexibility and time saving characteristics. Using locally available wire wrap services the two boards used in the interface were wired in one week. Insertion of the integrated circuits (IC) was all that was required to prepare the boards for testing. The wire wrap construction permitted modifications to be made by simply unwrapping the appropriate wires and installing the new wires. This is important since the design of the interface was based on assumed characteristics and it was expected that evaluation of the data would indicate the nature of modifications to be incorporated.

Since the logic circuitry of the interface was constructed using wire wrap techniques, the buffer circuitry, A/D convertors and indicator drivers were also constructed using these techniques. Double copper clad vector boards with .100 inch hole spacing were used. Wire wrap sockets were used for the IC's and A/D convertors. Discrete components were mounted using vector stand off pins. Cable connections were made using a header pin assembly similar to the wire wrap boards.

In the circuit diagrams to be presented next, the gates and logic circuits are identified using the identification scheme provided on the wire wrap boards. Two boards were used and are designated Board 1 and Board 2. As mentioned earlier each board had two IC socket groups. These are designated on the boards as Group A and Group B. Within each group the sockets are numbered from one to thirty. The pins for each socket are individually numbered from one to sixteen. The header pins for each group are identified as J1 and J2.

To identify a particular circuit connection, a six character reference code is used. The first character is the board number. The second character identifies the group. The next two characters specify either the socket number or the jack designator. The last two characters give the pin number. For example, a reference to 1A30-01 specifies board 1, group A, IC 30, pin 1.

On the circuit diagrams each gate or logic symbol has a circled number near it. This is the IC socket number. Each line connected to the symbol has a number near it which is the socket pin number. It should be noted that since all the sockets have sixteen pins, IC pin numbers 8 through 14 on fourteen pin IC packages correspond to socket pin numbers 10 through 16. This correspondence has been incorporated into the circuit diagrams so that any pin number reference is to the pin number on the wire wrap board not the IC. The group and board number for the circuit diagram are indicated as a note on each

diagram. Should an IC be used which is located in another group, the correct group letter is shown as a prefix to the IC number. Header pin connections are also prefixed by the appropriate group letter. Interconnections between boards are made only through the header pins. The interconnections are listed in Appendix B.

C. Circuit Module Description

Each circuit module of the digital interface will now be described. The circuit diagram and a timing diagram, where applicable, will be presented. A block diagram of the modules and control signals is shown in Fig. 1. The operation of each module will be explained using these diagrams. Unless otherwise specified the periods and repetition rates shown on the timing diagrams have nominal values. In these diagrams the relationship between the different signals is more important than the actual timing. The exact timing values are given in the text.

In each diagram the standard symbols are used for the logic gates. For special functions the symbols shown in Fig. 2 are used. A one shot multivibrator, SN74121 is shown in Fig. 2a. There are three inputs, B, A1, and A2. The one shot fires on the positive edge (0 to 1 transition) of a signal at the B input when A1 or A2 or both are grounded. The one shot also fires on the negative edge (1 to 0 transition) of a signal at A1 or A2 with B in the "1" state. These are the only conditions under which the one shot will fire. The pulse length at the output Q and complemented output $\overline{Q}$, is determined by the external resistor and capacitor.

A dual D flip flop with preset and clear, SN7474 is shown in Fig. 2b. Each flip flop contains a clocked D flip flop which transfers the input to the output while the clock, C, is high. Each flip flop also has a preset, P, and clear, C, input which overrides any input being clocked in through the D input. Thus each flip flop has a clocked D flip flop and an unclocked RS flip flop with a common output. To describe the state of the output, the set or clear reference is made with respect to the Q output.

Figure 2c shows a four bit binary counter, SN7493. This counter contains two independent counters. The A_{in} and A output form a divide by 2 counter. The B_{in} and B,C,D outputs form a divide by 8 counter. These two counters are both controlled by the reset inputs R_{01}, R_{02}. The counters are enabled only when R_{01} and R_{02} are grounded. Otherwise both counters are reset to zero. The counters both increment on the negative transition of the input. These are the commonly used IC's used in the interface. Other special purpose IC's will be described when they appear.

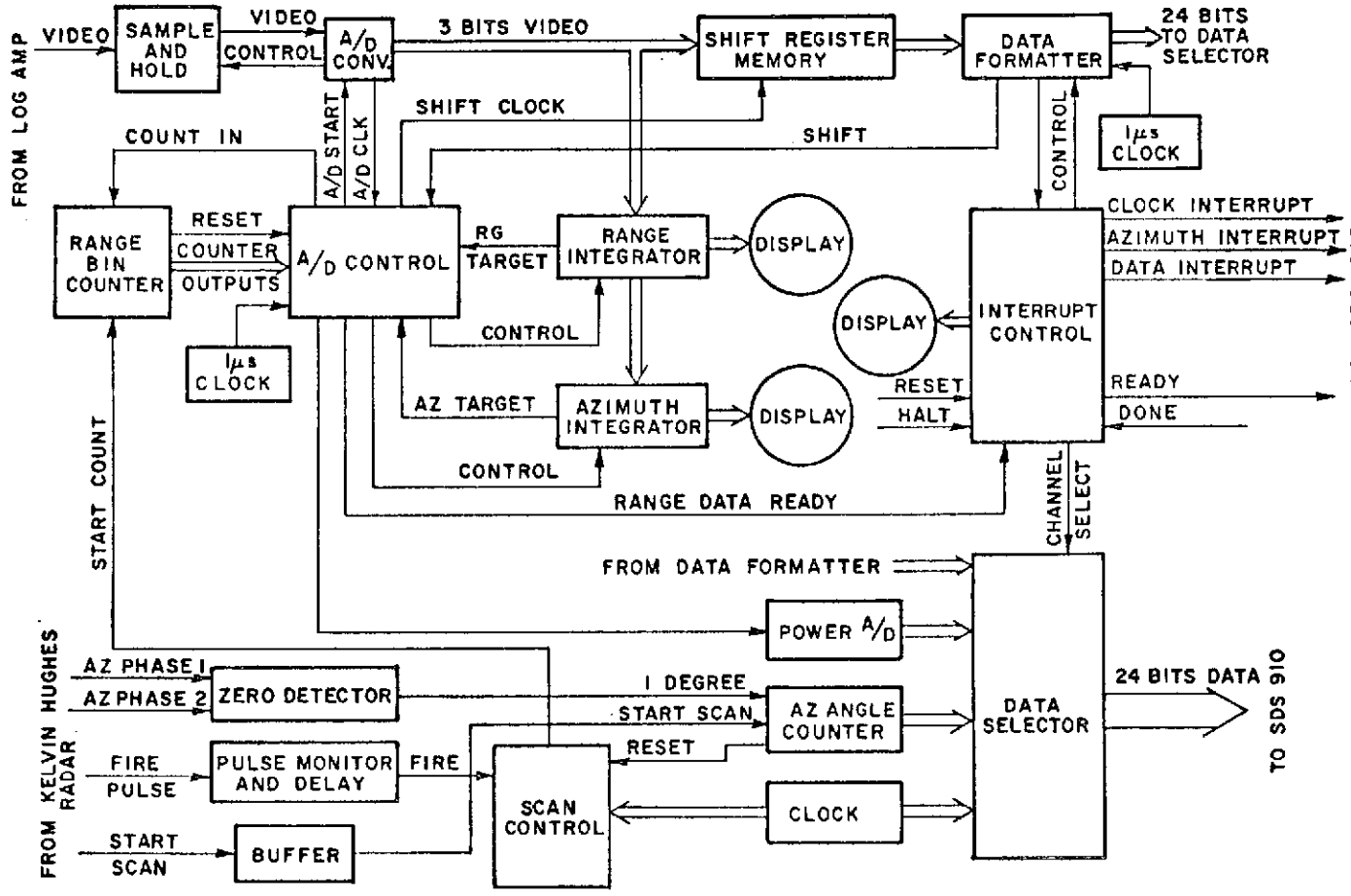
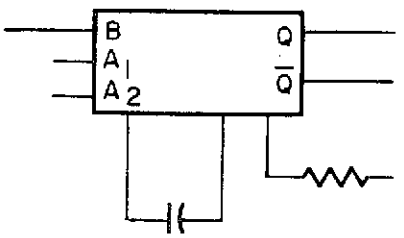
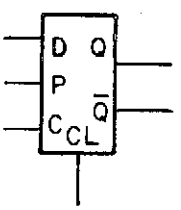


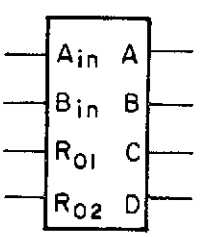
Fig. 1. Interface Block Diagram.



(a) ONE SHOT MULTIVIBRATOR



(b) FLIP FLOP



(c) FOUR BIT BINARY COUNTER

Fig. 2. Logic symbols for digital interface.

C-1. Scan control module: The scan control module initiates the operation of the other interface modules. The circuit diagram is shown in Fig. 3 and the timing diagram in Fig. 4. Operation is initiated when the minutes portion of the time ends in a three or an eight. This choice was made because this particular clock output is unambiguous. The value of the units digit in the time is decoded by the SN7442 BCD to decimal convertor, 1A03. The positive edge of the signal from 1A13-10 fires the one-shot 1A01. The output 1A01-06 resets the scan counter 1A09 and the azimuth target flag, TRGT FLG RST. The "1" from 1A03-10 enables the scan start signal, AZSTRT, to reset the divide by eight counter 1A05 through 1A02-03. In this reset state the scan counter 1A09 has a count of zero.

The first state of the scan control module is entered when the antenna begins a scan after the reset has occurred. This is signaled by AZSTRT at 1A02-01 and 1A02-04. The output from 1A02-03 increments the scan counter 1A09. Thus, the B output is "1" and the C and D outputs are "0". The output from 1A07-12 is "1" so the output from the divide by eight, 1A05-13, appears at 1A04-13. This signal has a positive transition every 10 ms and is used to initiate the digitization of the video return for one look angle. The 10 ms period permits the antenna to scan slightly more than one beamwidth between digitizations.

The next AZSTRT pulse increments the scan counter 1A09 and the B input goes to "1". After the first scan either or both the B and C outputs are high. This is used to signal the rest of the interface that these scans are data scans to be recorded. (Recall that the first scan is used to determine whether a target is present anywhere in the scan.) The succeeding scans are used for recording data. The computer software requires five scans to record the radar return of a complete scan. Thus, when six scans have been used, the digitization is to be terminated. On the sixth scan the counter output is B=0, C=1, D=1. Thus, the output from 1A02-13 is "1" and the output from 1A07-12 is "0". This shuts off the STARTCT output from 1A04-13 and the counter input 1A02-06.

C-2. A/D control module: The A/D Control Module controls the digitization and storage of the video return, the integration of the return in range and azimuth and the initiation of the computer interrupt. The circuit diagram is shown in Fig. 5. This module has three states which are determined by the outputs of the Range Bin Counter Module. These states are represented by the signals 1CT, one range bin digitized; 101CT, one hundred one range bins digitized and 134CT, one hundred thirty four range bins digitized. Also obtained from the Range Bin Counter are a RESET and $\overline{\text{RESET}}$ which are reset signals.

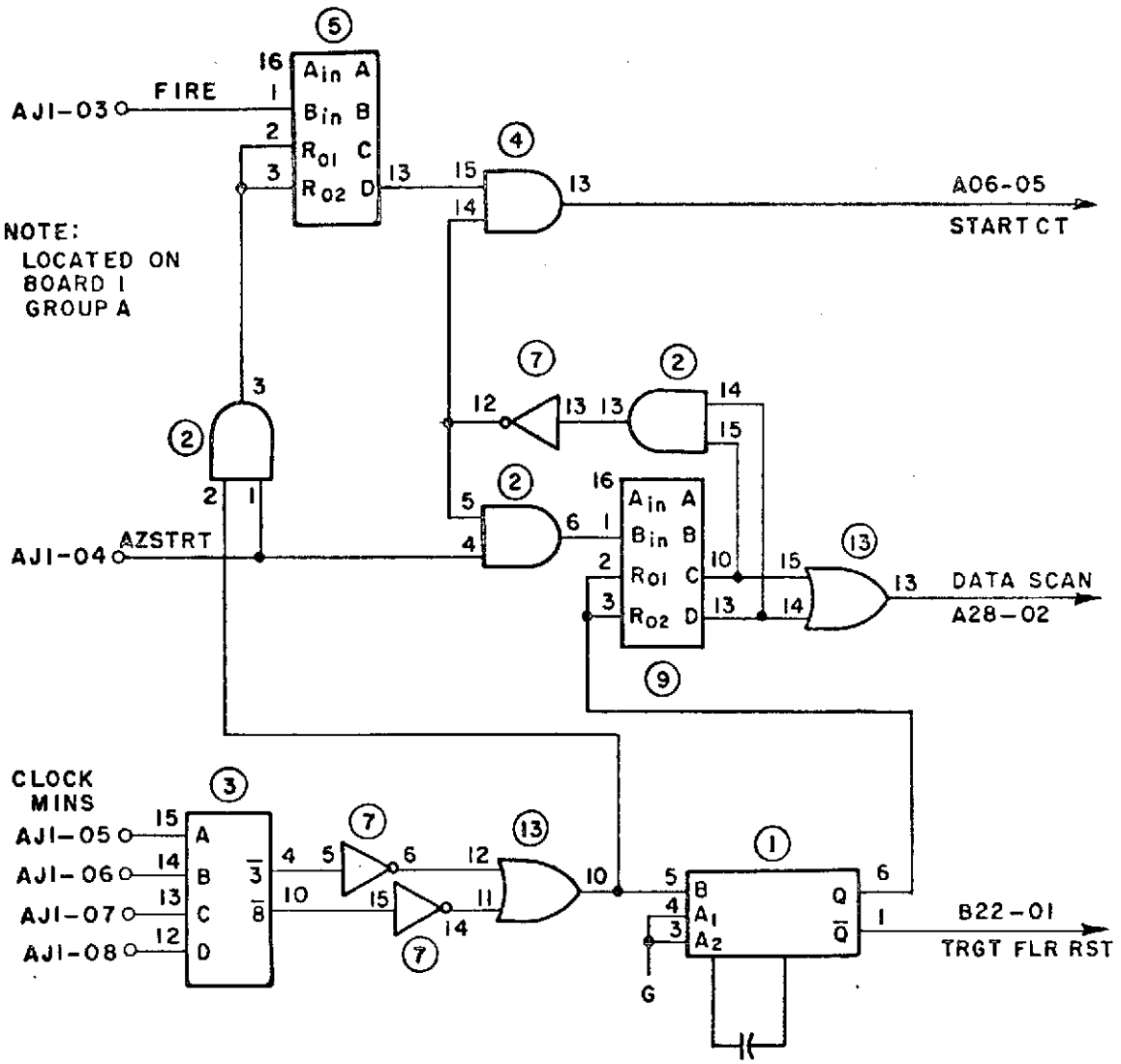


Fig. 3. Scan Control Module.

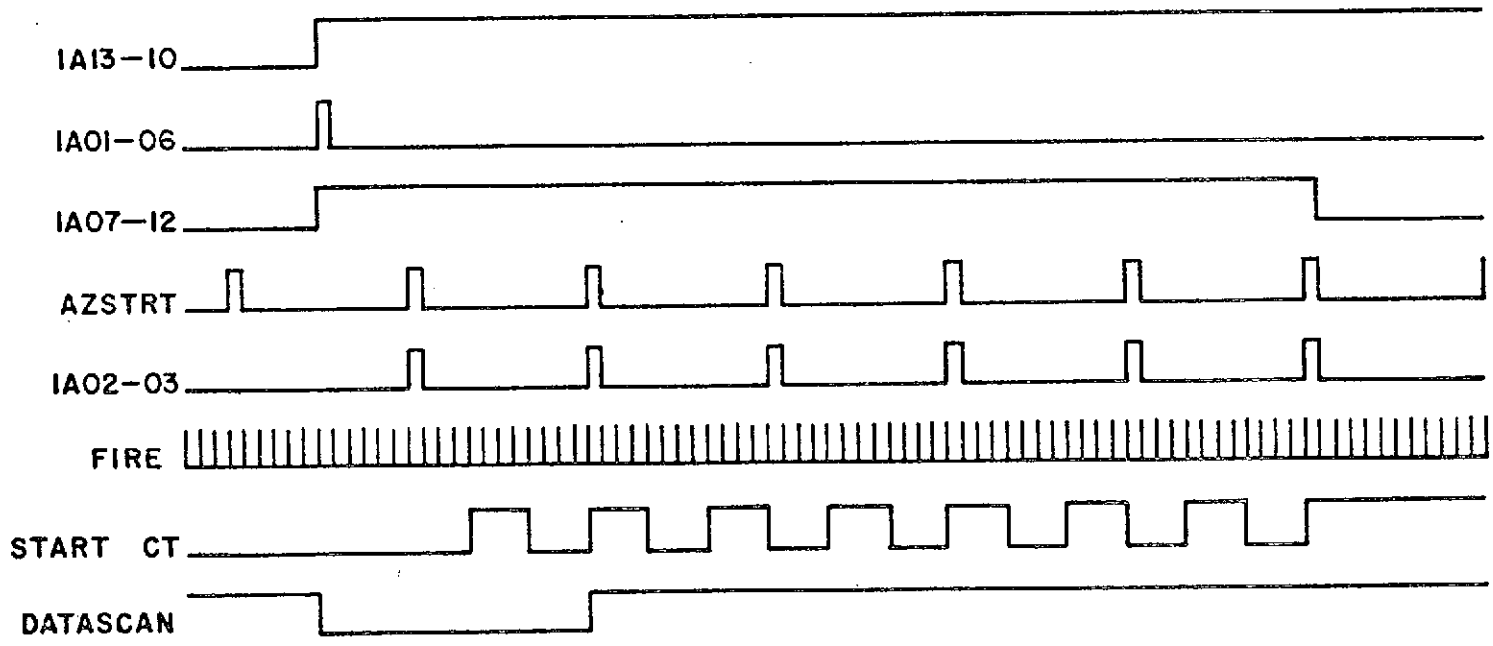


Fig. 4. Scan Control Timing.

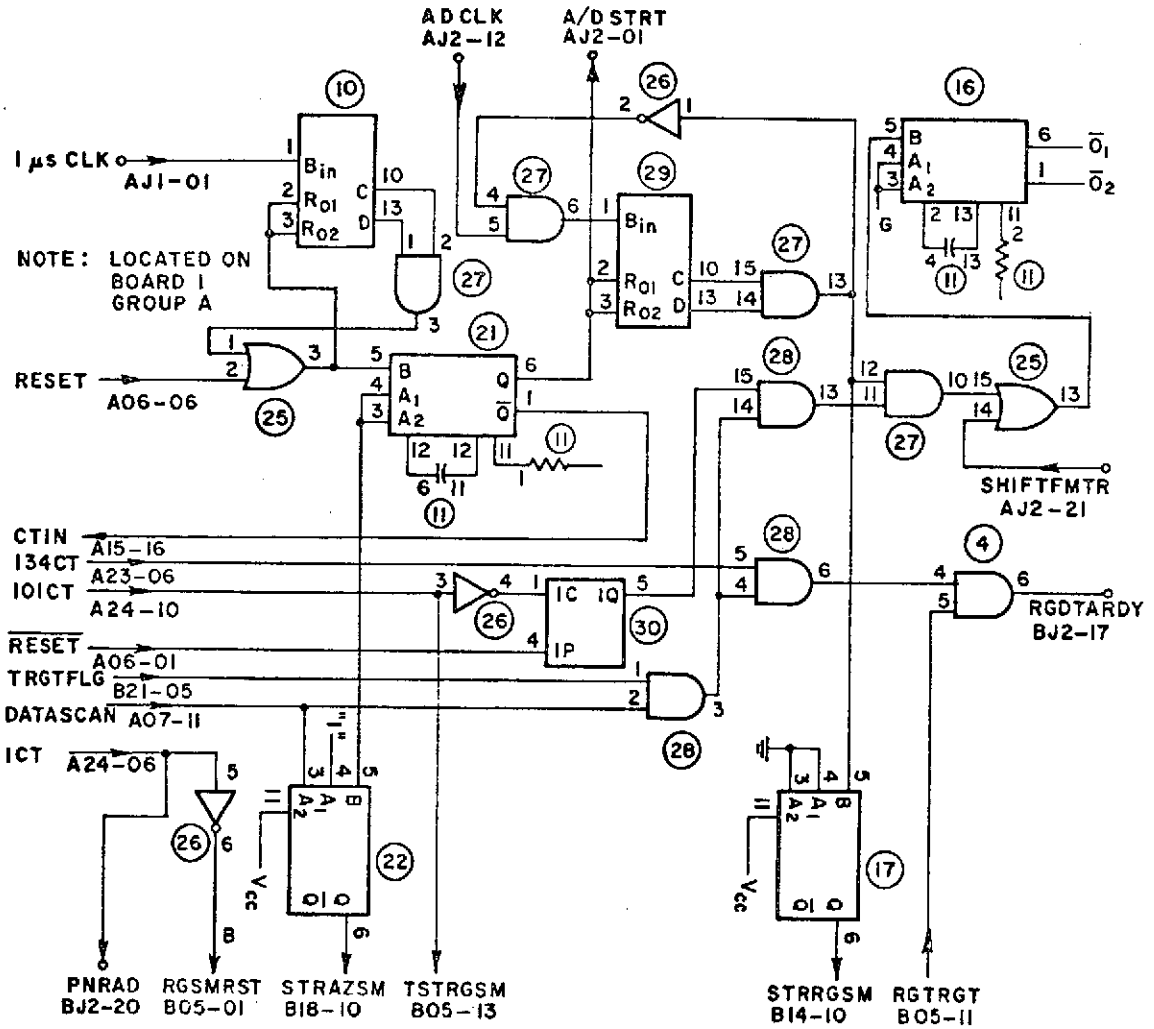


Fig. 5. A/D Control Module.

An eight bit, successive approximation A/D converter and a sample and hold are used for the digitization. The A/D converter determines the value of each bit successively, beginning with the most significant bit. One bit is determined every 500 ns, thus the three bit conversion used here requires 1.5 μs. The sample and hold amplifier has a 10 ns aperture time and a DC to 500 KHz bandwidth to the 3 dB point. The amplifier settles within 0.1% of the final value in 1 μsec or less.

The digitization process starts when a reset pulse is received from the Range Bin Counter. This fires one shot 1A21 which resets the A/D clock pulse counter, 1A29 and increments the Range Bin Counter. An A/D convert signal, A/$\overline{\text{DSTRT}}$ is sent to the A/D convertor. The complement reset pulse, $\overline{\text{RESET}}$, presets the flip flop 1A30. The output 1A30-05 gates the DATASCAN·TRGTFLG signal from 1A28-03 to 1A28-13. This gate is used to control the memory shift command through 1A27.

After six clock pulses from the A/D convertor are counted by 1A29, the output at 1A27-13 goes high. This disables the input to the counter through 1A27-06 and sends a shift command to 1A27-12. If there is an azimuth target and if the scan being digitized is a data scan, then 1A27-11 is high and the shift command is sent to 1A16-05. The positive edge fires the one shot which generates the proper two phase clock signal for the Shift Register Memory. The positive edge of the shift command from 1A27-13 also fires one shot 1A17. This updates the current range integration sum with the data from the present range bin. The Range Bin Counter is incremented at the start of a range in digitization so the 1CT signal is used to reset the Range Integrator before the first range bin is added to the current sum.

To perform successive digitizations, the range bin timing counter, 1A10, must reach a count of six. The input to the counter is a pulse train with a 1 μs period so there is 6 μs between range bin digitizations. This counter and logic gate 1A27 determine the range bin size. To change the range bin size it is only necessary to change the circuitry for these two elements.

The digitization process continues to cycle until 100 range bins have been digitized. Since the Range Bin Counter has the count of the current range bin being digitized, a signal is generated for a count of 101, 101CT. This clears the flop flop 1A30 which disables the shift command from reaching the clock generator through 1A27. The range target flag is also tested at this time by TSTRGSM.

On the one hundred-thirty fourth range bin, 134CT goes high. This disables the one shot 1A21 through the A1,A2 inputs. If the azimuth sum store one shot has been enabled by DATASCAN being a "0", then the positive edge of 134CT causes the current sum in the Range Integrator to be added to the current azimuth sum by STRAZSM. The

combination of gates 1A28-03, 1A28-06 and 1A04-06 determine if there is a range target, an azimuth target and if this is a data scan. If so then the range data ready signal RGDTARDY goes high. This signals the Interrupt Control that the digitized range bins are ready to be sent to the computer.

The logic descisions made in the A/D Control Module are best summarized by the equations below. Signals having no identifying name are identified by the pin number where they appear.

$$1A27\text{-}10 = 1A27\text{-}13[101CT \cdot (TRGTFLG \cdot DATASCAN)]$$
$$SHIFT = 1A27\text{-}10 + SHIFTBFFR$$
$$RGSMRST = 1CT$$
$$STRRGSM = 1A27\text{-}13$$
$$TSTRGSM = 101CT$$
$$A/DSTRT = RESET + 1A27\text{-}03$$

C-3. Interrupt Control Module

The Interrupt Control Module controls the transfer of data from the interface to the parallel input buffer on the SDS 910 computer using three levels of priority interrupt. As mentioned earlier, the number of interrupts used could be reduced to one if necessary. The changes needed will be described later in this section. The circuit diagram is shown in Fig. 6.

For the purposes of this section it will be more convenient to refer to logic signals as being active or inactive. The reason for this is that the buffers used to drive the cables to the computer invert the signals. Secondly, some of the computer signals are inverted by the buffers which receive them. The actual voltage levels of 0 and 5 volts are shown in the timing diagram in Fig. 7.

Operation of the interrupt control is initiated on the positive edge of the RGDTARDY signal from the A/D Control Module. This fires the one shot 2B23 which produces a 700 ns pulse. The positive edge clocks 2B18-06, 2B19-06, 2B19-10 and 2B18-10 into an inactive state. This assures that all interrupts are cleared and the paralled input buffer (PIB) is signaled that the data is not ready. The state counter 2B30 is reset by the positive pulse. The inverted pulse from 2B23-01 overrides the clocked data which activates the second priority interrupt, $\overline{\text{INTER2}}$, and PIB ready signal, READY. The INTER2 signal sets the data selector to the clock output so the PIB receives the clock data when a parallel input (PIN) instruction is executed by the computer. The Interrupt Control Module is now in state 0 as shown in the state diagram, Fig. 8, and the timing diagram, Fig. 7.

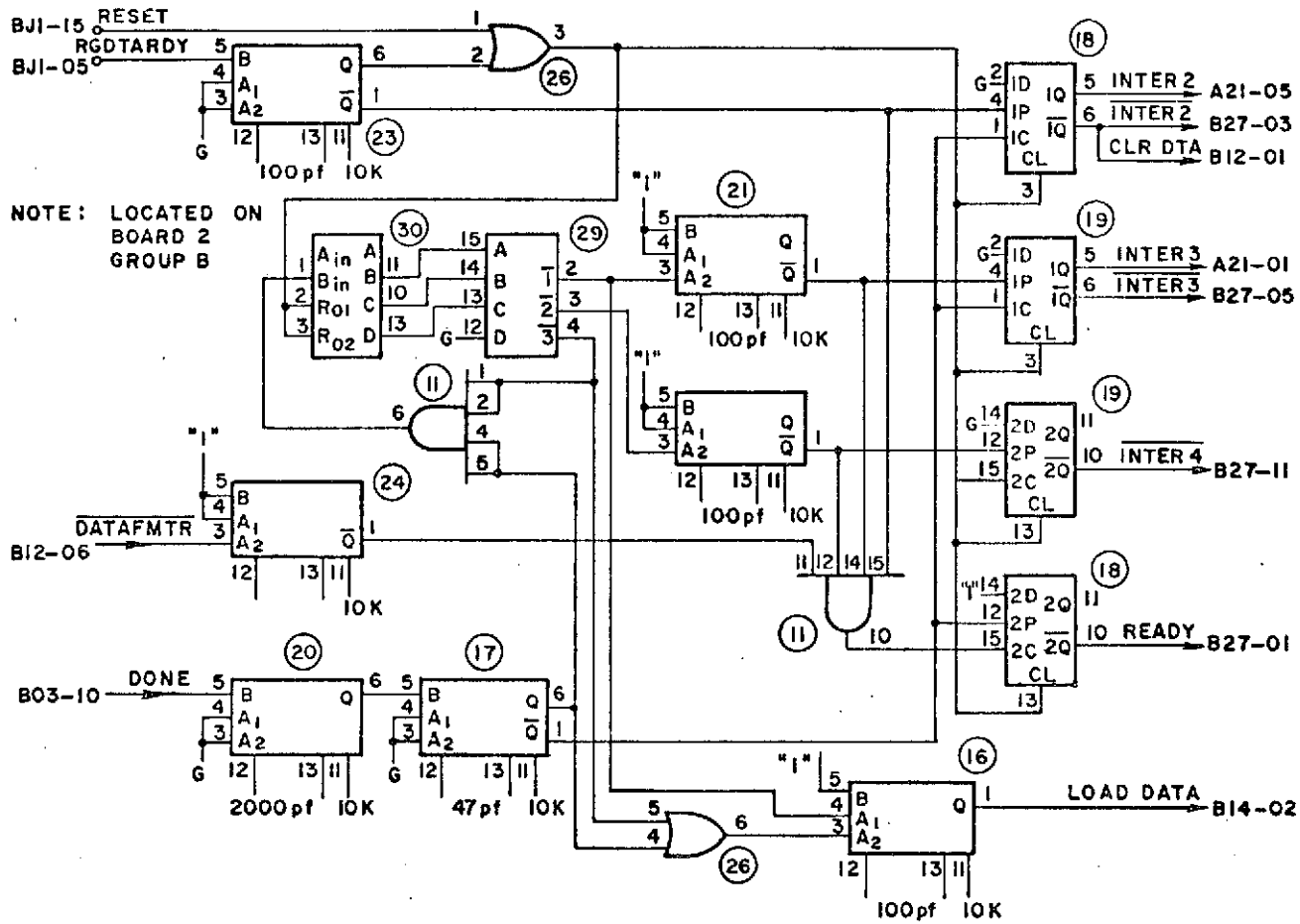


Fig. 6. Interrupt Control Module.

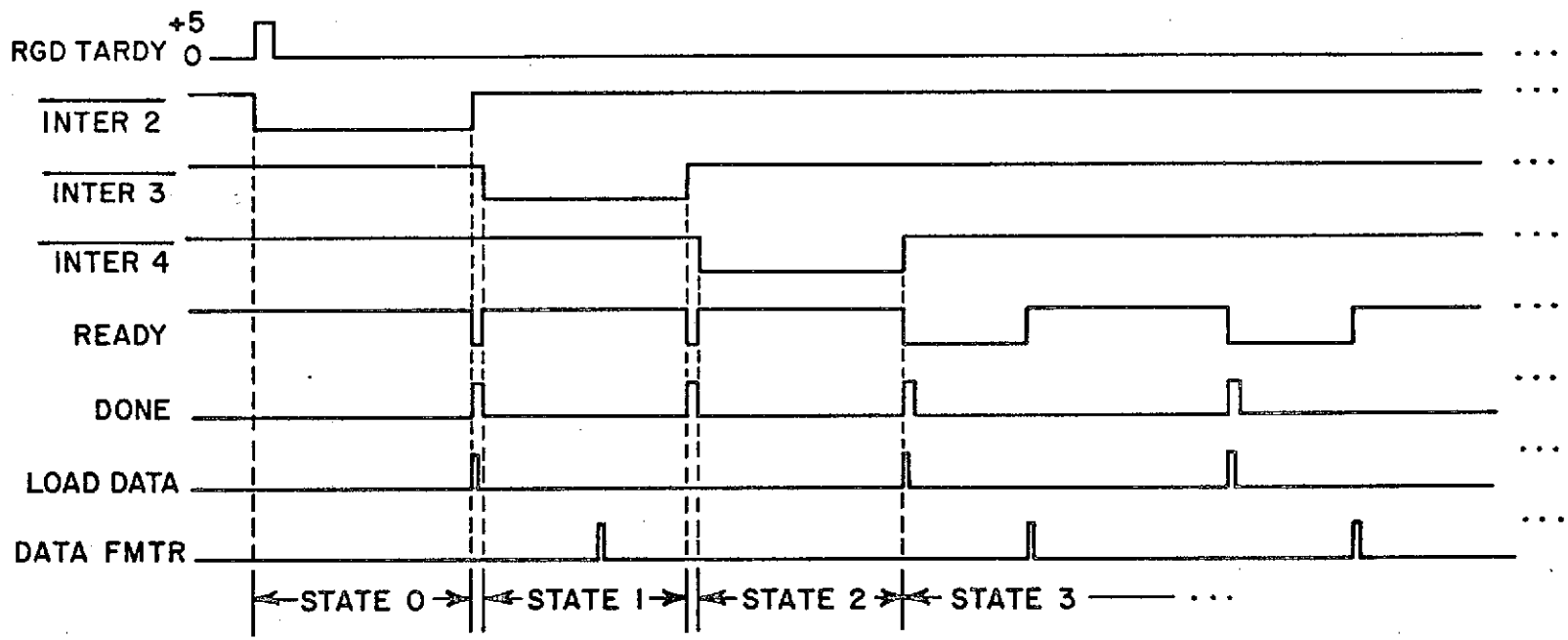


Fig. 7. Timing Diagram.

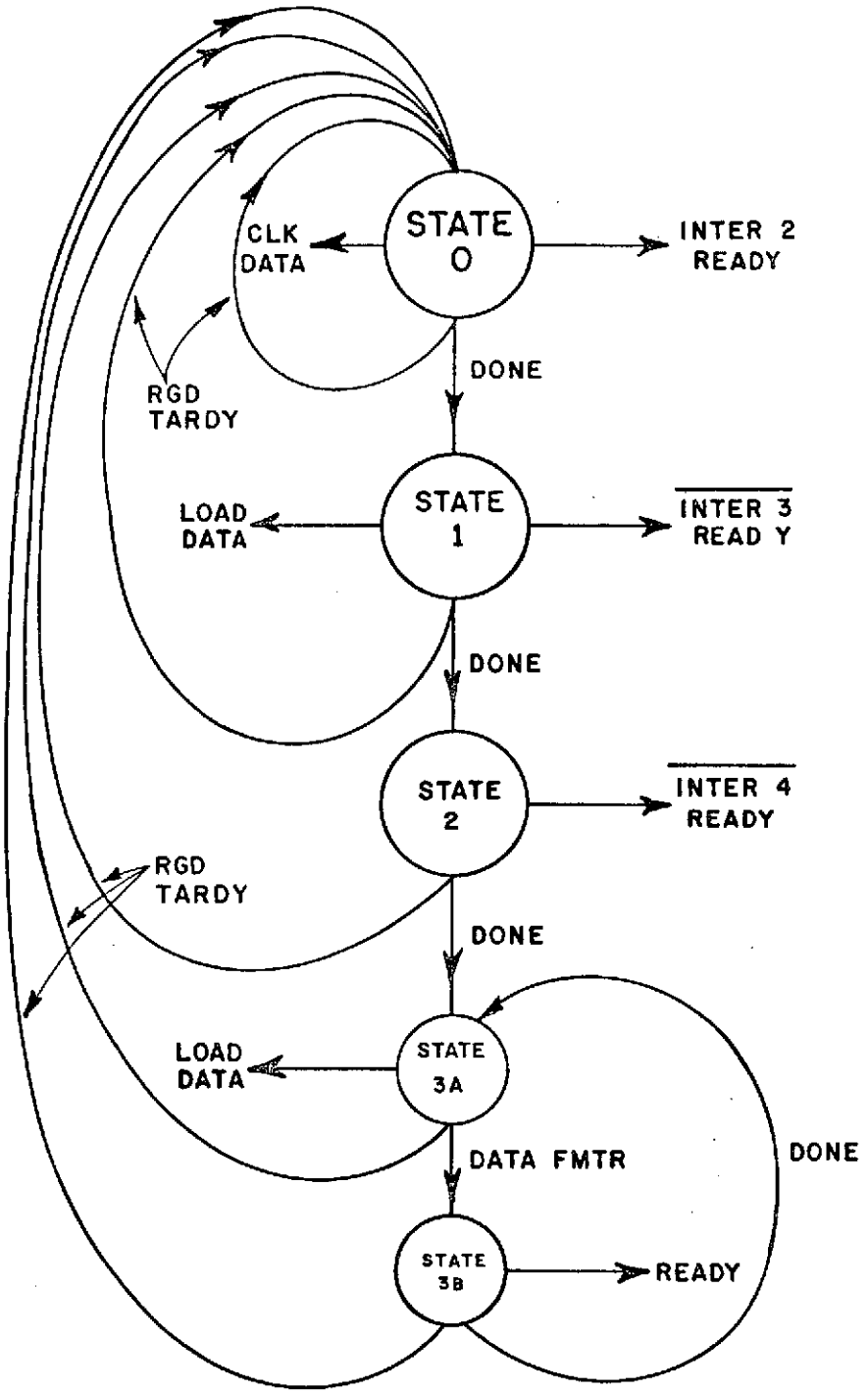


Fig. 8. Interrupt Control Status.

The computer program services the interrupt with a PIN instruction. At the completion of this instruction the PIB sends an input complete signal, DONE, to the interface. This fires the one shot 2B20 which has a long enough duration to prevent noise on the DONE signal from re-triggering the one shot. For controlling the module a second one shot is used, 2B17 which produces a pulse 300 ns wide. This pulse inactivates the interrupts and the READY signal. The state counter 2B30 is incremented by the inverted output and the state one line 2B29-02 is activated. This fires the one shot 2B21 which produces a 700 ns pulse. The next interrupt, $\overline{\text{INTER3}}$, is activated and the ready signal becomes active. The INTER3 signal sets the data selector to the azimuth and transmitted power data. To prepare the video data for input on the next interrupt, one shot 2B16 is also fired which initiates the operation of the Data Formatter Module with the LOADDTA signal. The Data Formatter responds 6 μs later with an operation complete signal, DATAFMTR which attempts to activate the READY signal. Since READY is already active this is ignored. Thus, the Interrupt control is in state 1 as shown in Figs. 7 and 8.

The computer program acknowledges the interrupt with a PIN instruction and a DONE signal is received upon completion of the parallel input process. The interrupts and ready signals are inactivated by the pulse from 2B17 and the state counter is incremented. The state two line becomes active and one shot, 2A28 is fired. The lowest priority interrupt becomes active, $\overline{\text{INTER4}}$ along with READY. The data selector is set to the formatted video which was prepared earlier and the interface waits in state 2.

When the computer responds with the execution of the PIN instruction and DONE signal, the interrupts and READY signal are inactivated. A load data signal, LOADDTA is sent to the formatter. The interface is now in state 3A. The READY signal becomes active when a DATAFMTR signal is received. This moves the Interrupt Control to state 3B.

Once the Interrupt Control enters state 3 further input to the state counter is disabled at 2B11-06. A DONE signal from the computer after the PIN causes another word of video data to be prepared by the Data Formatter and a READY signal issued. Thus, the Interrupt Control cycles between states 3A and 3B until a RGDTARDY signal is received which initializes the operation. A total of 12 PIN instructions in state 3 are required to read all the video data from the interface.

As mentioned earlier, it is possible to input all the data from the interface using only one interrupt to signal the computer input process. The interrupt outputs from the Interrupt Control are connected to drivers. To use only one interrupt first remove the three connections from the interrupt flip flop to the drivers. Next connect $\overline{\text{INTER2}}$ to the

buffer for the interrupt level desired. When this interrupt is received by the computer, fifteen consecutive PIN instructions will input the clock, azimuth and video data. The data will arrive in the same order as before. Fifteen PIN instructions are required.

C-4. Range Integrator and Azimuth Integrator Modules

The Range and Azimuth Integrators both use the same design. The input for the Range Integrator comes from the video A/D convertor. Eight bits from the Range Integrator are used by the Azimuth Integrator as input. The two integrators are shown in Figs. 9 and 10.

The integrator circuit uses a ten bit parallel adder composed of two 4 bit adder IC's and a 2 bit adder IC. The sum is fed back to one of the adder inputs through a parallel access register. The data is transferred only on the positive edge of a clock pulse. This prevents the current sum from propagating through the adder again and destroying the true sum. The registers also have a clear line so that the integrator can be reset to zero.

The target flags for each integrator use a delay flip flop. When the flag detector input at 1B21-01 in the Azimuth Integrator and 1B21-03 in the Range Integrator goes high the flag is set. The range target flag detector input is connected to a test bit in the Range Integrator sum. The azimuth flag detector input is connected to the output of the ten bit magnitude comparator shown in Fig. 11. For the range detector, seven bits of the range sum are brought out on a 14 pin header plug located at 1B25. The detector input 1B25-05 is connected to the appropriate bit on this header. The comparator input appears at 1B26-02 to 1B26-06 and 1B26-10 to 1B26-14. A "1" appears at 1B26-01 and a zero at 1B26-07. Thus, the threshold value can be set on the header by the interconnections of 1B26-01 and 1B26-07 to the computer inputs. Changes in the flag thresholds are easily made using the headers.

In both integrators the test bit goes through an AND gate into the preset input on the target flip flop. When the integrators are reset both flip flops are reset. After the test bit goes high the complementary output of the flip flop goes low and prevents any other input from changing the flip flop. The Range Integrator has a second flip flop connected as a delay flip flop. This flip flop is used to clock the target flag to the output RGTRGT on the range bin count of 101. This prevents a target which is outside the fifty mile range from setting the flag.

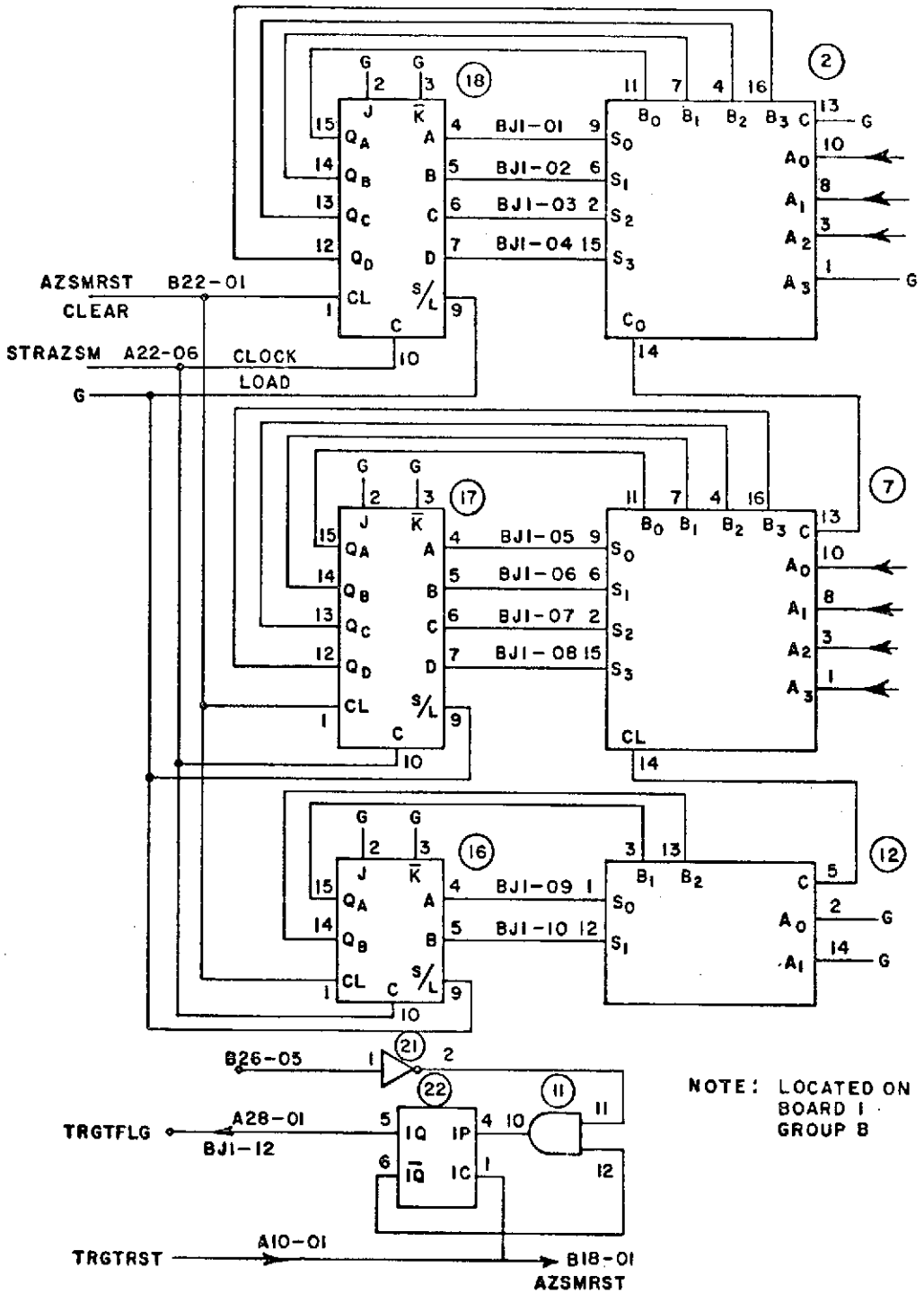


Fig. 9. Azimuth Integrator.

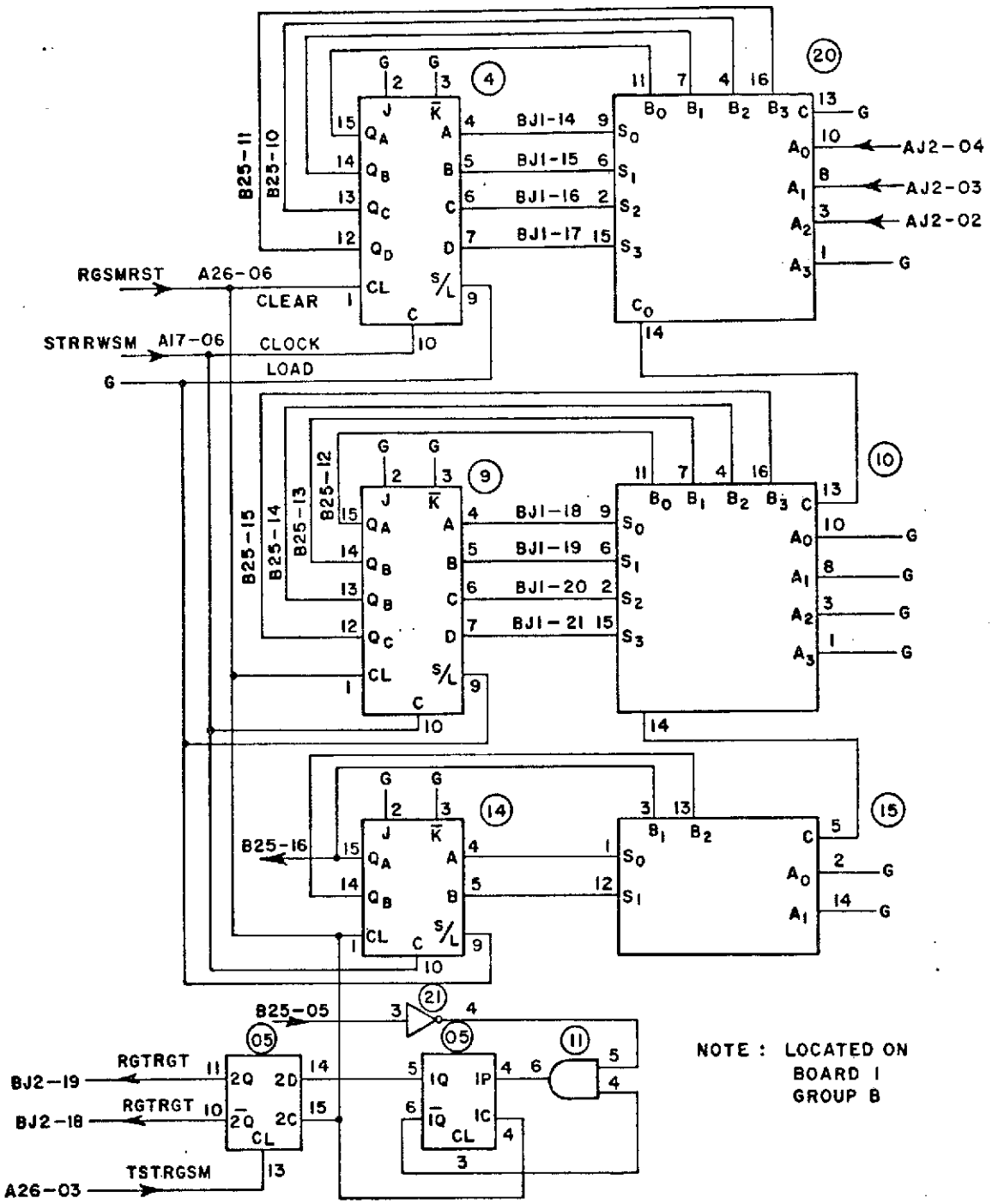


Fig. 10. Range integrator.

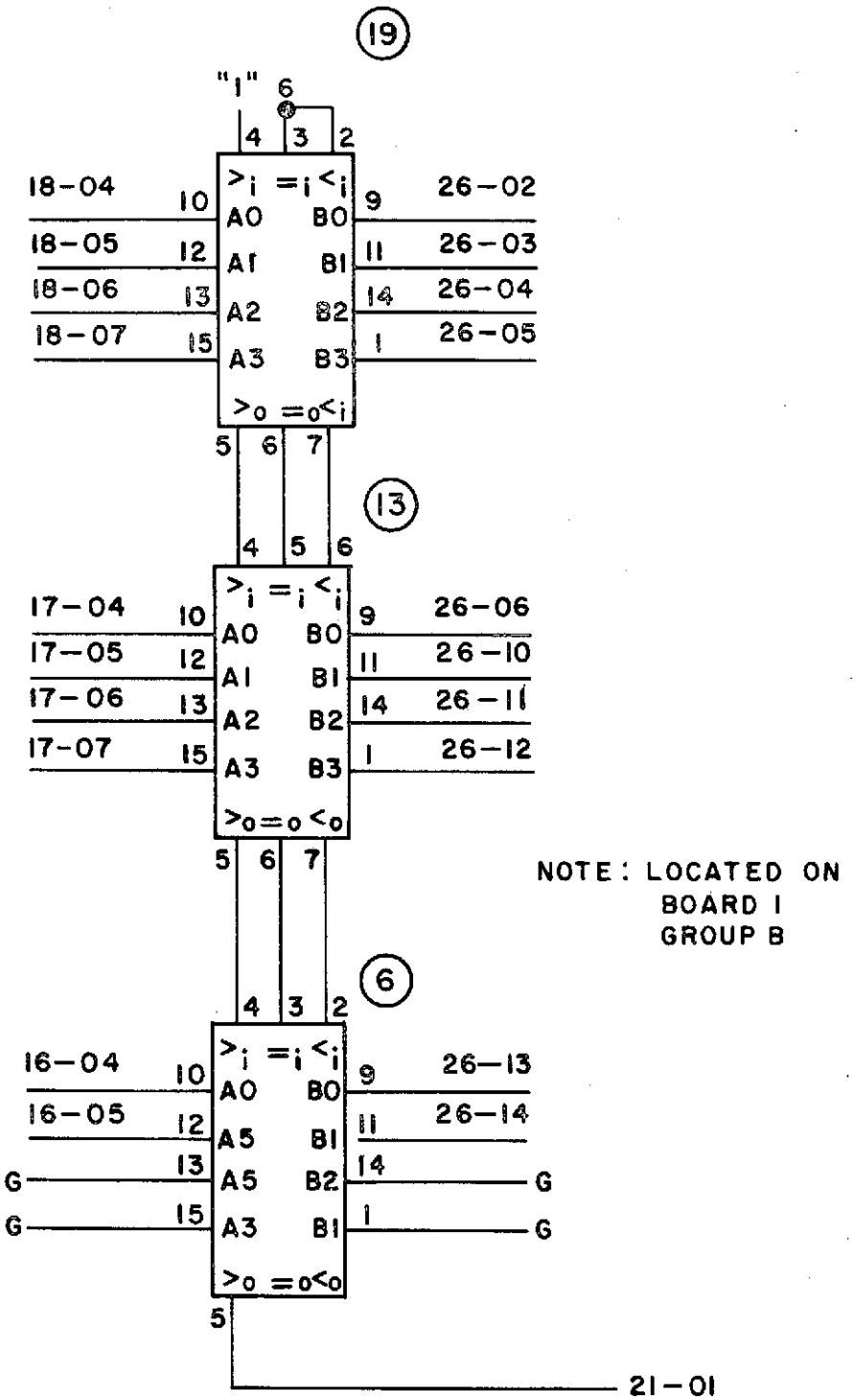


Fig. 11. Azimuth integrator target detector.

The signals which control each integrator are:

Range Integrator

RGSMRST = Resets range integrator and target flag
STRRGSM = Stores current sum in parallel access register
TSTRGSM = Clocks target flag to target flag output
RGTRGT = Range target flag output

Azimuth Integrator

AZSMRST = Resets azimuth integrator and target flag
STRAZSM = Stores current sum in parallel access register
TRGTRST = Resets target flag
TRGTFLG = Azimuth target flag output

They are shown in the circuit diagrams, Figs. 9 and 10.

C-5. Data Formatter Module

For efficient data transfer between the computer interface and the 3 bit video data words are packed into 24 bit words for computer input. The circuit diagram is shown in Fig. 12 and the timing diagram in Fig. 13. The key to the formatter operation is the fact that the data from the shift register memory appears at the high to low transition of the phase two clock pulse, ϕ_2. This is shown in the timing diagram with a dashed line.

Operation is initiated when the LOADDTA signal resets the clock pulse counter, 2B14. The clock input to latch 2B05 goes high since the count is zero. The latch receives the current output from the shift register. The next pulse from the 1 μs CLK increments the counter and sends a shift command to the shift register, SHIFTFMTR, through the A/D Control Module. The timing diagram shows that the data appears at the shift register output approximately 700 ns after the clock pulse. This insures that data is not loaded into the wrong latch.

Successive clock pulses continue the process until a count of eight is reached. On the eighth pulse the data in the formatter is ready and the ready signal, DATAFMTR, goes low when flip flop 2B-12 is reset by the $\overline{8}$ output from 2B15-10. The shift register is shifted on the eighth pulse to ready the first video data word for the next formatting cycle. The ninth clock pulse disables the counter input through 2B13-02. A shift pulse is not sent since the counter increments on the negative pulse transition. So, by the time the shift command is enabled at 2B13-04, the input 2B13-03 is low.

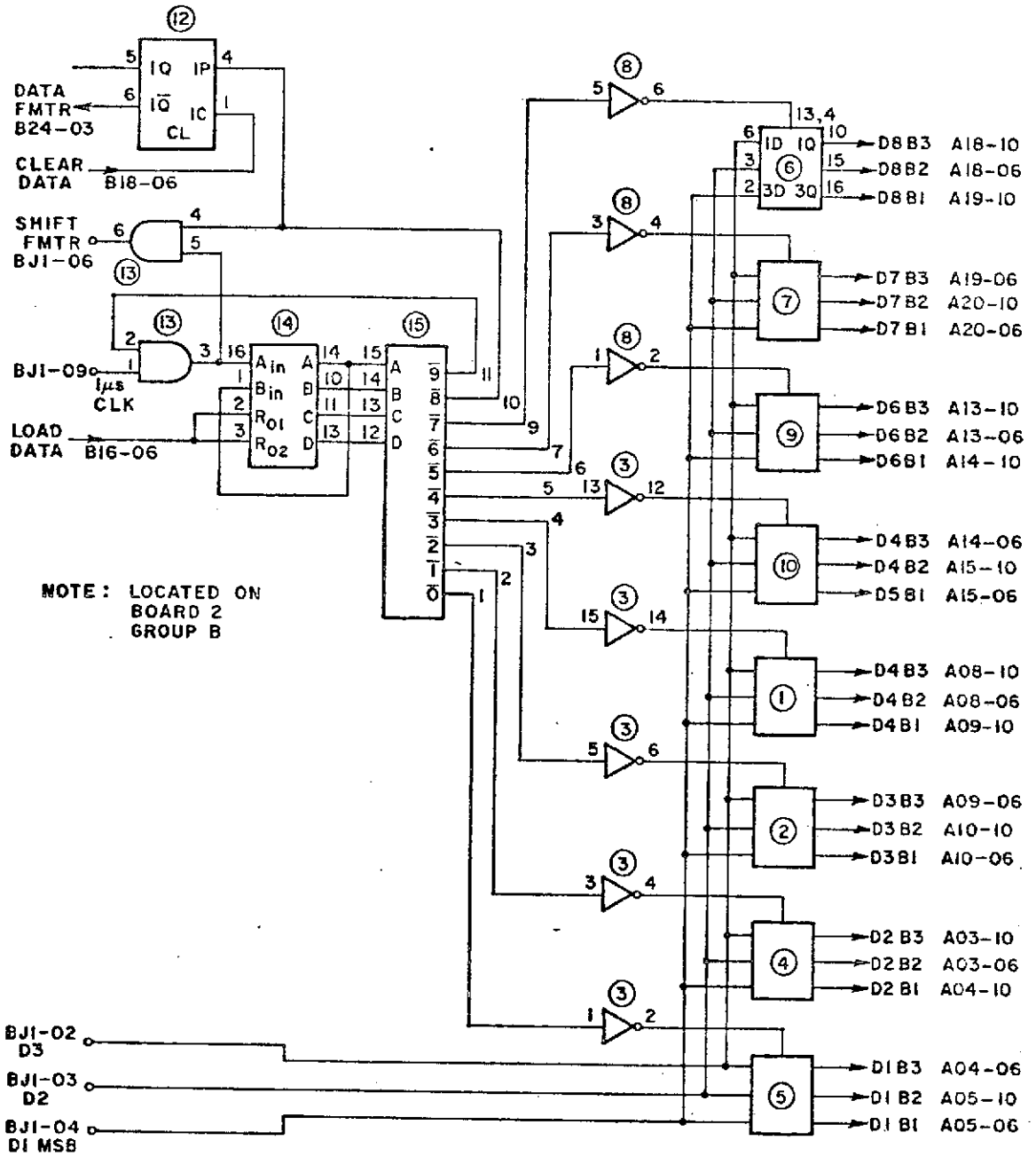


Fig. 12. Data formatter.

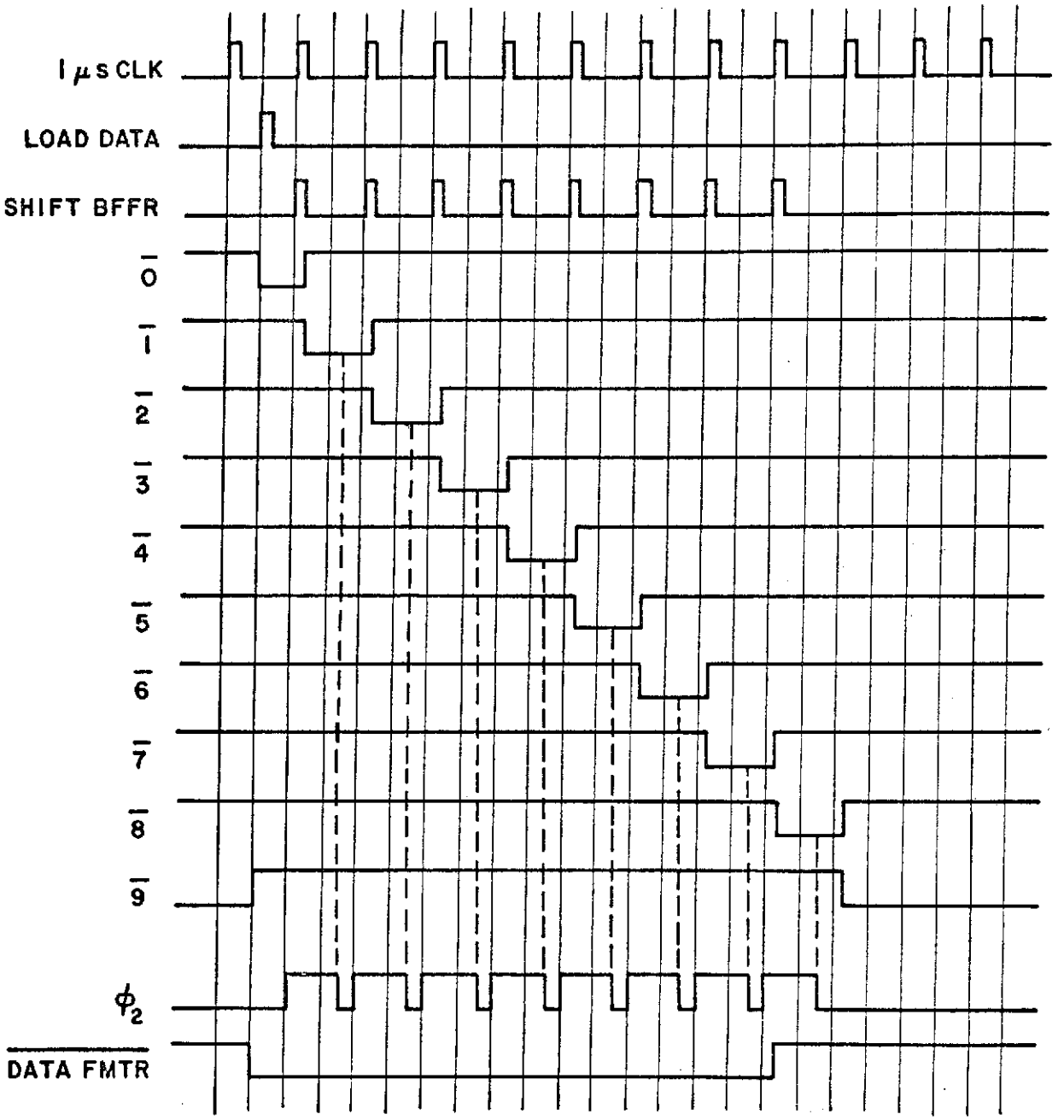


Fig. 13. Timing diagram for data formatter.

C-6. Range Bin Counter Module

The Range Bin Counter Module is used to indicate the range bin currently being processed by the A/D Control Module. The circuit shown in Fig. 14 uses three 4 bit binary counters in a binary coded decimal counter configuration. Counter 1A15 is the unit's digit, 1A14 is the ten's digit and 1A12 is the hundred's digit. The one shot 1A06 is used to reset the counters and the A/D Control Module as described earlier. The desired counts 1CT, 101CT and 134CT described earlier are detected by gates 1A18, 1A19, 1A20, 1A23, and 1A24. The detection is best explained by the logic equations below.

(1) $$1CT = [\ \overline{(HA+HB)}\cdot\overline{(HC+HD)}\ ]\cdot[\ \overline{(TA+TB)}\cdot\overline{(TC+TD)}\ ]\cdot\overline{(UB+UC+UD)}\cdot UA$$

(2) $$101CT = HA\cdot[\ \overline{(TA+TB)}\cdot\overline{(TC+TD)}\ ]\cdot\overline{(UB+UC+UD)}\cdot UA$$

(3) $$134CT = HA\cdot TB\cdot TA\cdot UC$$

The H, T and U prefixes denote the hundred's digit, ten's digit and unit's digit respectively. The A, B, C and D suffixes denote the counter outputs. It is recognized that for the 134CT there is an ambiguity if the counter increments past 134. However, the signal 134CT disables the counter input signal in the A/D Control Module so this cannot occur.

C-7. Data Selector Module

The Data Selector multiplexes four channels of data into the 24 drivers for the Parallel Input Buffer. Only three channels are used currently as shown in the circuit diagram in Fig. 15. The channel assignments are shown below and the data inputs are shown in Table III.

TABLE III

DATA SELECTOR CHANNEL ASSIGNMENTS

Channel 0	Video data from data formatter		
Data Selector	Data Source	Description	
A05-06	B05-16	Word 1	bit 1
A05-10	B05-15		bit 2
A04-06	B05-10		bit 3
A04-10	B04-16	Word 2	bit 1
A03-06	B04-15		bit 2
A03-10	B04-10		bit 3
A10-06	B02-16	Word 3	bit 1
A10-10	B02-15		bit 2
A09-06	B02-10		bit 3
A09-10	B01-16	Word 4	bit 1
A08-06	B01-15		bit 2
A08-10	B01-10		bit 3
A15-06	B10-16	Word 5	bit 1
A15-10	B10-15		bit 2
A14-06	B10-10		bit 3
A14-10	B09-16	Word 6	bit 1
A13-06	B09-15		bit 2
A13-10	B09-10		bit 3
A20-06	B07-16	Word 7	bit 1
A20-10	B07-15		bit 2
A19-06	B07-10		bit 3
A19-10	B06-16	Word 8	bit 1
A18-06	B06-15		bit 2
A18-10	B06-10		bit 3

TABLE III (Contd)

Channel 1	Clock day-time code		
Data Selector	Data Source	Description	
A05-05	AJ1-25	Clock hundred days	2's bit
A05-11	-24		1's bit
A04-05	-23	Clock ten days	8's bit
A04-11	-22		4's bit
A03-05	-21		2's bit
A03-11	-20		1's bit
A10-05	-19	Clock unit days	8's bit
A10-11	-18		4's bit
A09-05	-17		2's bit
A09-11	-16		1's bit
A08-05	-15	Clock ten hours	2's bit
A08-11	-14		1's bit
A15-05	-11	Clock unit hours	8's bit
A15-11	-10		4's bit
A14-05	-09		2's bit
A14-11	-08		1's bit
A13-05	-07	Clock ten minutes	4's bit
A13-11	-06		2's bit
A20-05	-05		1's bit
A20-11	-04	Clock unit minutes	8's bit
A19-05	-03		4's bit
A19-11	-02		2's bit
A18-05	-01		1's bit
A18-11	-GND		

TABLE III (Contd)

Channel 2	Azimuth and power monitor		
Data Selector	Data Source	Description	
A05-04	A22-11	Azimuth angle	256's bit
A05-12	A23-13		128's bit
A04-04	-10		64's bit
A04-12	-11		32's bit
A03-04	-14		16's bit
A03-12	A24-13		8's bit
A10-04	-10		4's bit
A10-12	-11		2's bit
A09-04	-14		1's bit
A09-12	GND		
A08-04	GND		
A08-12	A25-01	Power A/D	
		most significant bit	bit 1
A15-04	-02		bit 2
A15-12	-03		bit 3
A14-04	-04		bit 4
A14-12	-05		bit 5
A13-04	-15		bit 6
A13-12	-14		bit 7
A20-04	-13	least significant bit	bit 8
A20-12	GND		
A19-04	GND		
A19-12	GND		
A18-04	GND		
A18-12	GND		

CHANNEL 0	Formatted video data
CHANNEL 1	Clock output code
CHANNEL 2	Azimuth angle and power monitor
CHANNEL 3	Not used

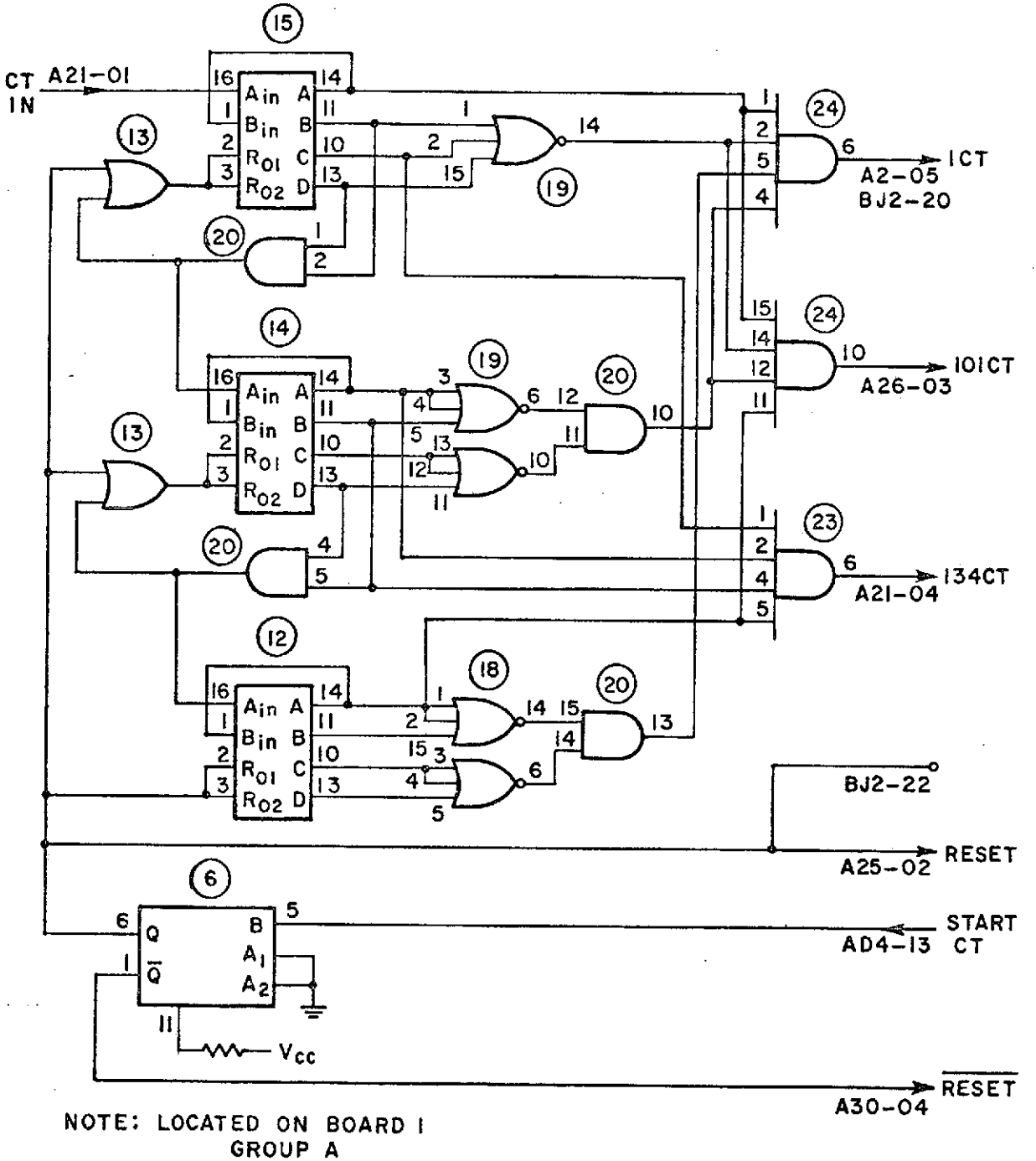


Fig. 14. Range bin counter.

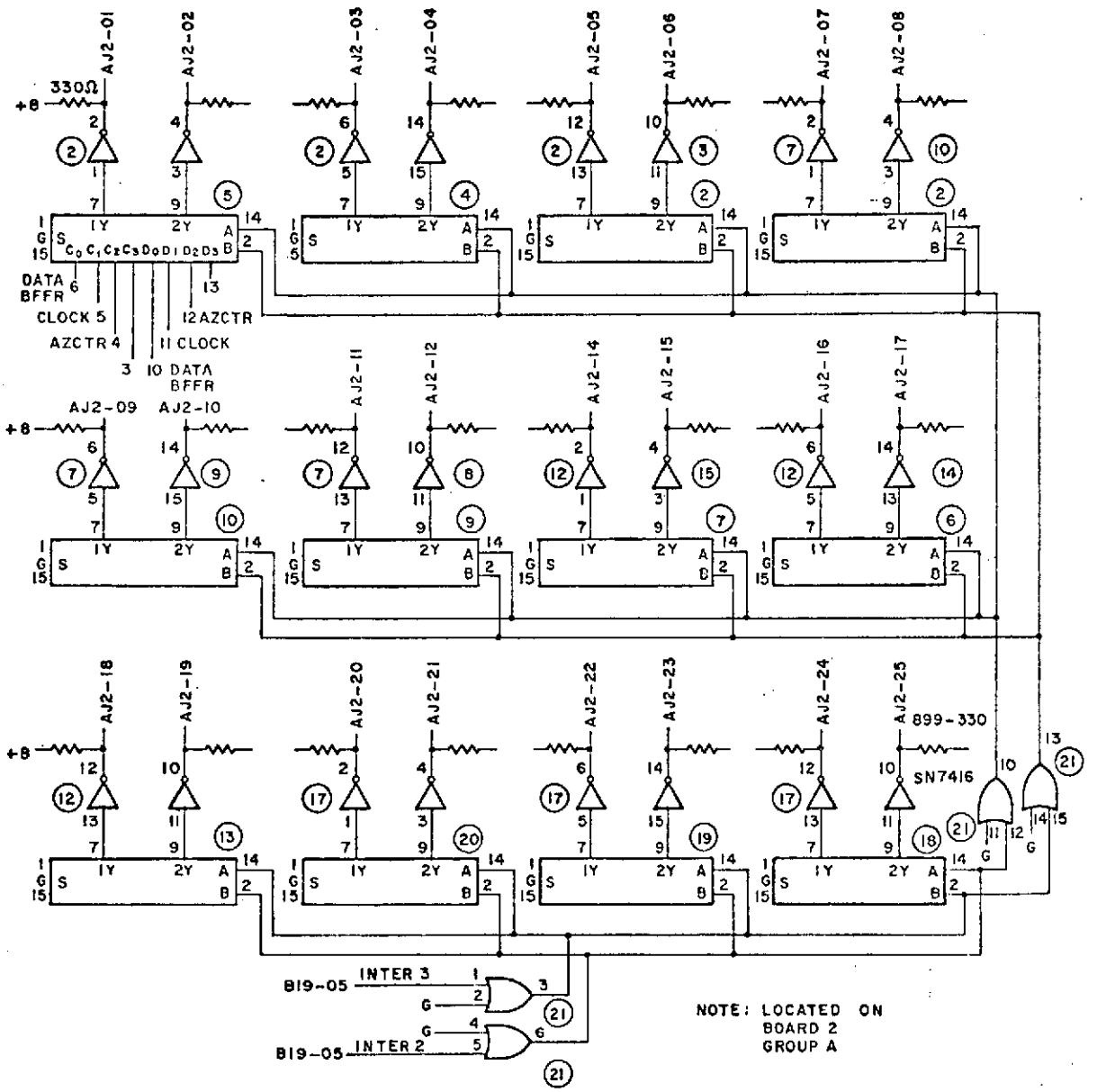


Fig. 15. Data selector.

The channel selection is determined by the interrupt signals, INTER2 and INTER3. The channel select lines, A and B, receive a two bit control word as given below.

(4)	CHANNEL 0	A = INTER2 = 0 B = INTER3 = 0
(5)	CHANNEL 1	A = INTER3 = 1 B = INTER2 = 0
(6)	CHANNEL 2	A = INTER3 = 0 B = INTER2 = 1

Recall that INTER3 is the interrupt for azimuth angle and transmitted power data and INTER2 is the interrupt for clock data. The OR gate 2A21 is used as a selector line driver and to provide a means for selecting Channel 3 if required in the future. The select signal for Channel 3 should be connected to 2A21-02 and 2A21-04 after the grounds have been removed. The invertors connected to each data selector are drivers for the parallel input buffer.

C-8. Interrupt Buffer Module

Since the SDS 910 uses diode transitor logic, the output levels of the interface, 0 to 5 volts must be changed to 0 to 8 volts. This is done by open collector hex invertors. To receive the DONE signal from the parallel input buffer a zener diode is used on the input of an invertor. These circuits are shown in Fig. 16a.

C-9. Shift Register Memory

Two dual 100 bit MOS static shift registers are used to store the 3 bits of video data for each of the one hundred range bins. The circuit diagram is shown in Fig. 16b. The shift registers require two non-overlapping clock pulses, ϕ_1, ϕ_2, whose voltage levels are -12 to +5 volts. The discrete component circuitry at 1B22 and 1B23 is used to transform the 0 to 5 volt clock pulse to +5 to -12 volts. The circuitry is shown in Fig. 17.

The operation of the shift register is straightforward. To store data statically, ϕ_1 is held high (+5 volts) and ϕ_2 is held low (-12 volts). Data is loaded into the register when ϕ_1 is low and the register is shifted on the low to high transition of ϕ_1 and the high to low transition of ϕ_2. The output data appears on the high-low transition of $_2$. The clock phases must be non-overlapping which means that ϕ_1 and ϕ_2 cannot be below 3 volts simultaneously.

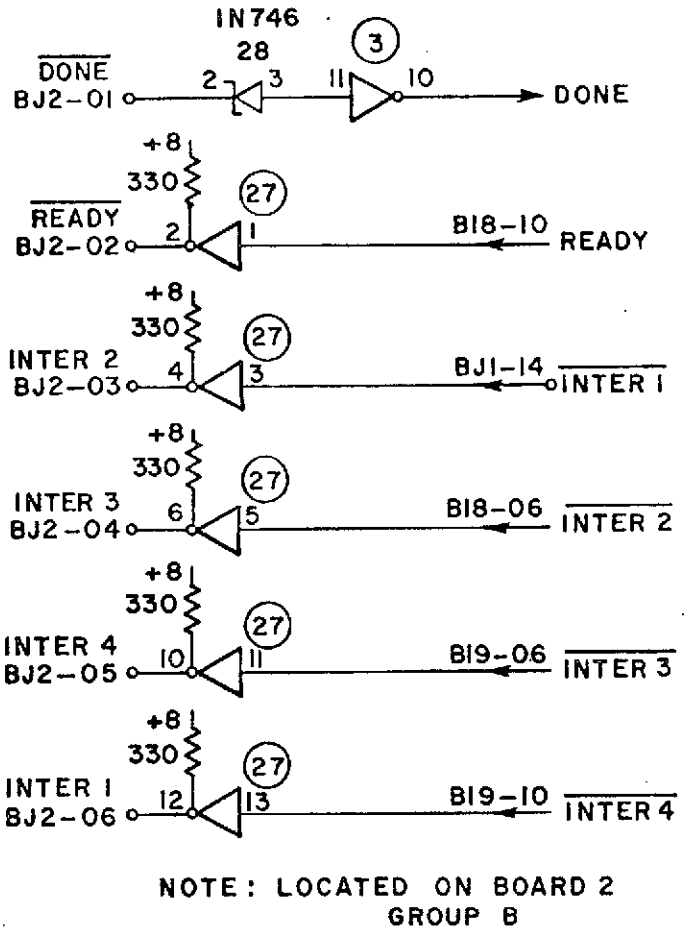


Fig. 16a. Interrupt buffer.

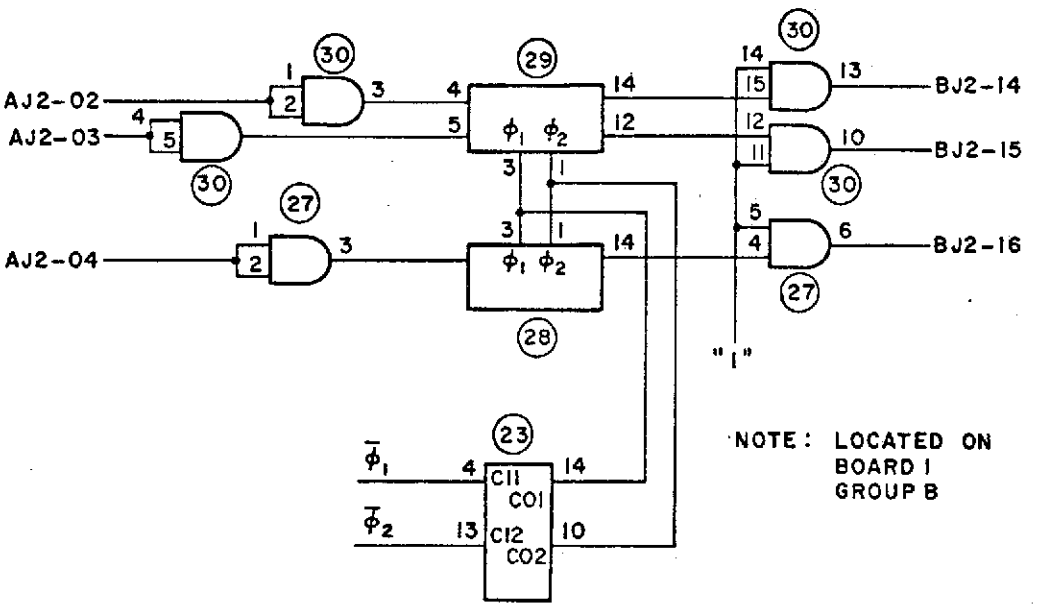


Fig. 16b. Shift register memory.

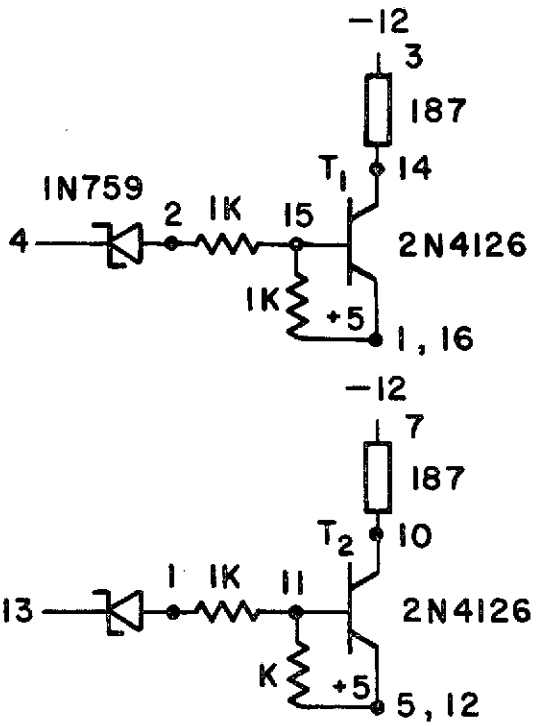


Fig. 17. Shift register clock drivers.

This condition is easily met in the drivers used in this circuit. In the static condition ϕ_1 is high which means that T_1 is on and ϕ_2 is low so that T_2 is off. When a shift pulse is received $\overline{\phi_1}$ and $\overline{\phi_2}$ both change state which means that T_1 and T_2 switch to opposite states. In the circuit used, the turn off time of the drive transistor is slower than the turn-on time due to the stored base charge. This protects the non-overlapping clock pulses. The actual pulse shapes of ϕ_1 and ϕ_2 are shown in Fig. 18. The cross over point is seen to be +4 volts which is safe.

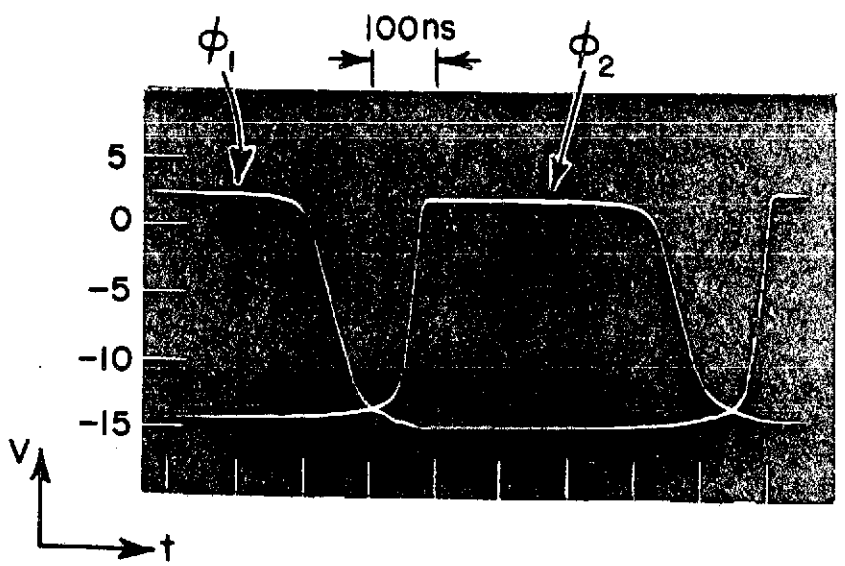


Fig. 18. Shift register clock waveforms.

C-10. 1 μs Clock Buffer Module

The 1 μs clock used in the interface was not directly compatible with TTL logic levels. An amplifier-buffer is used to produce a TTL level pulse and a one shot is used to form a narrow pulse train. The circuit is shown in Fig. 19.

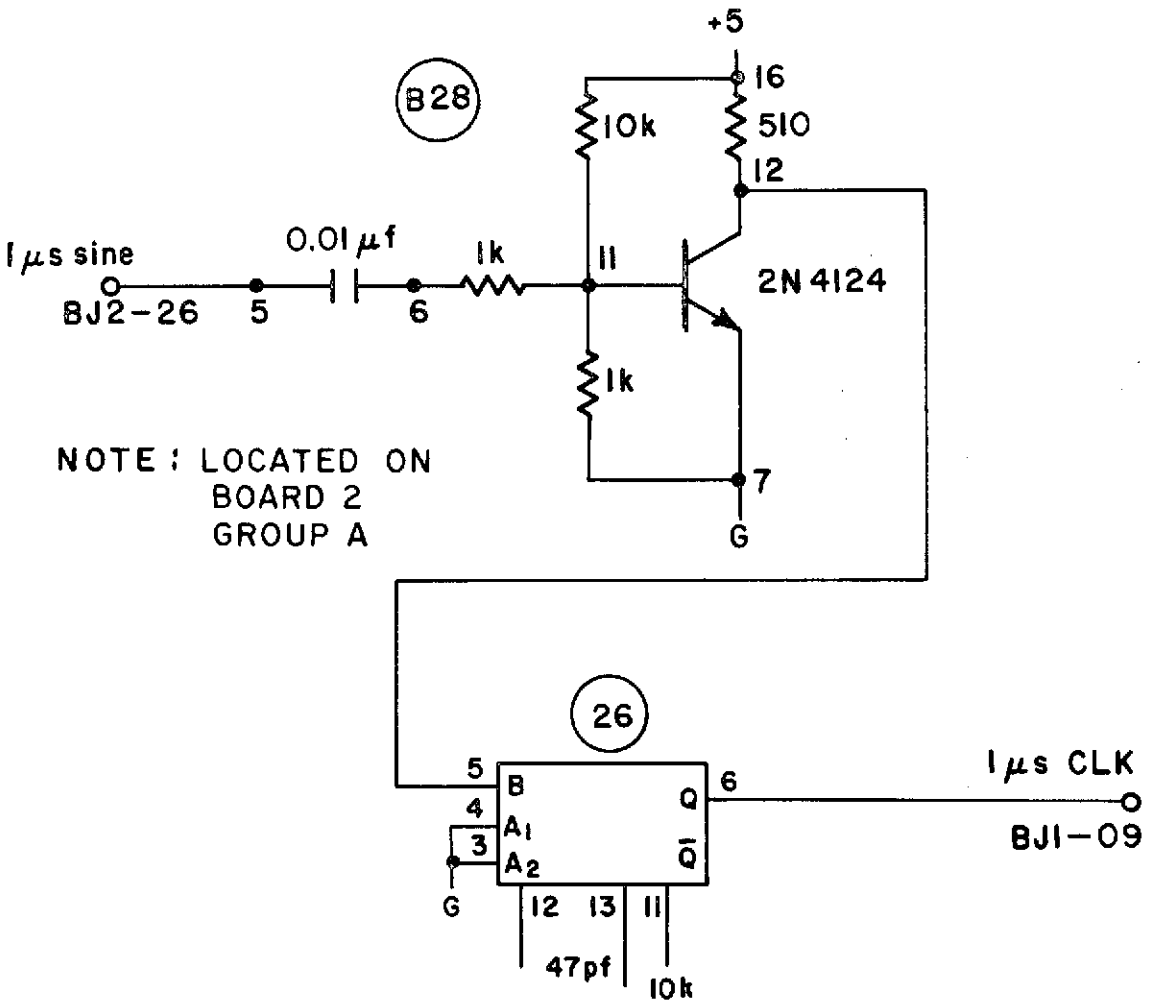


Fig. 19. 1 μs clock buffer.

C-11. Radar Fire Buffer Module

The detected radar pulse from the power monitor was not of sufficient level to drive TTL logic IC's. A small amplifier is used and shown in Fig. 20. A pair of one shots are used to delay the

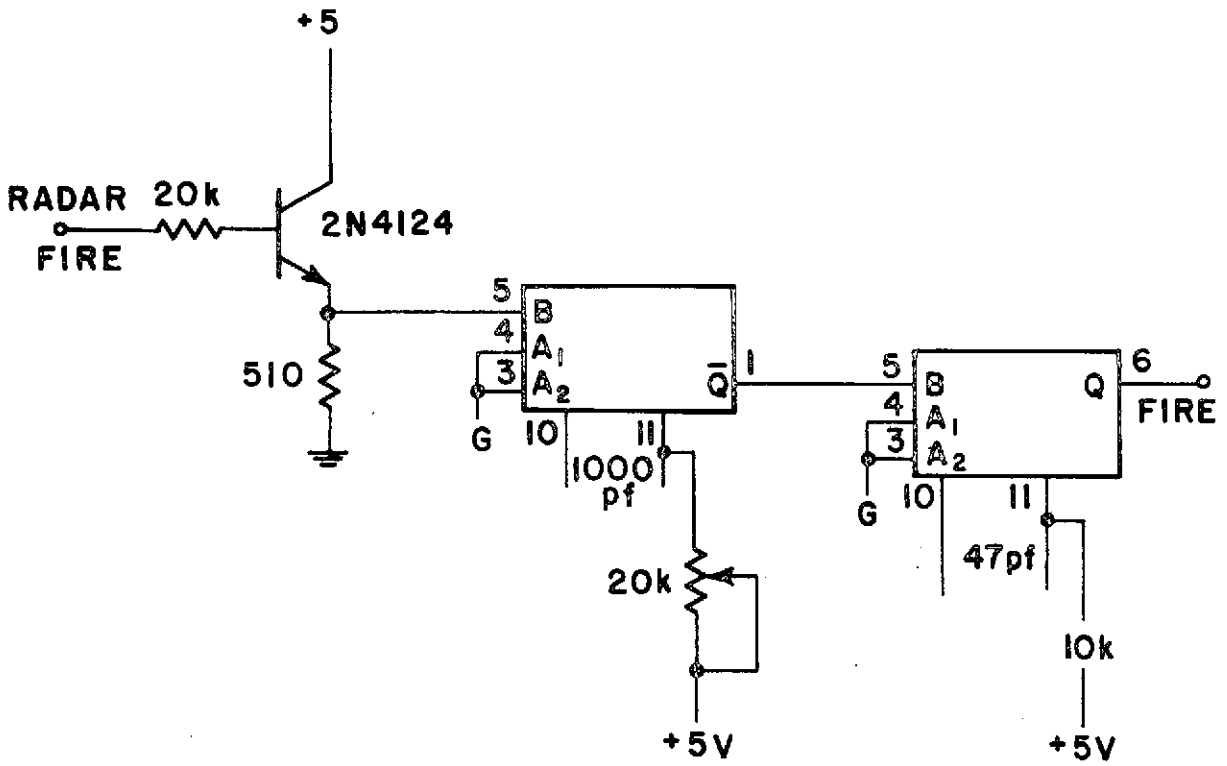


Fig. 20. Radar fire buffer.

output pulse to account for propagation delay. This delay can also be used to suppress ground clutter since the digitization starts when a FIRE pulse is received by the Scan Control Module.

C-12. Azimuth Angle Counter and Azimuth Angle Buffer Modules

The azimuth angle of the radar antenna is determined by counting the zero crossings of the two phase generator attached to the antenna. The Azimuth Angle Buffer shifts the voltage level of the heading line marker and produces a pulse train from the two phase zero crossings. The circuit diagram is shown in Fig. 21. The Azimuth Angle Counter Module is a binary counter which counts the input pulses as seen in Fig. 22. The one shots 2A30 and 2A28 are used to form the reset pulse, AZRST.

C-13. Display Drivers

The visual displays used in the interface are light emitting diodes (LED). These LED's are driven by open collector buffers and invertors as shown in Figs. 23, 24 and 25. The signals displayed are

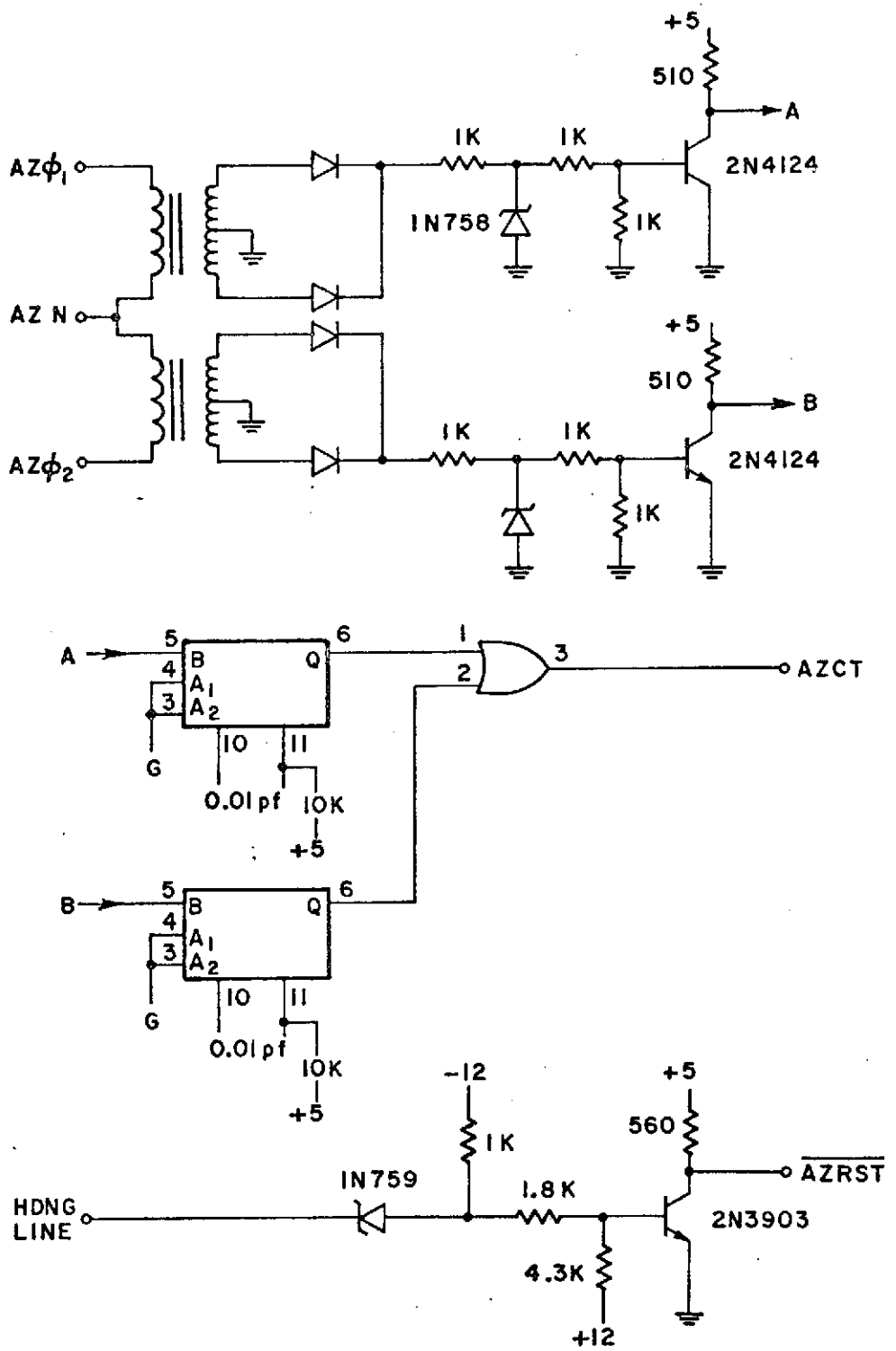


Fig. 21. Azimuth angle buffer.

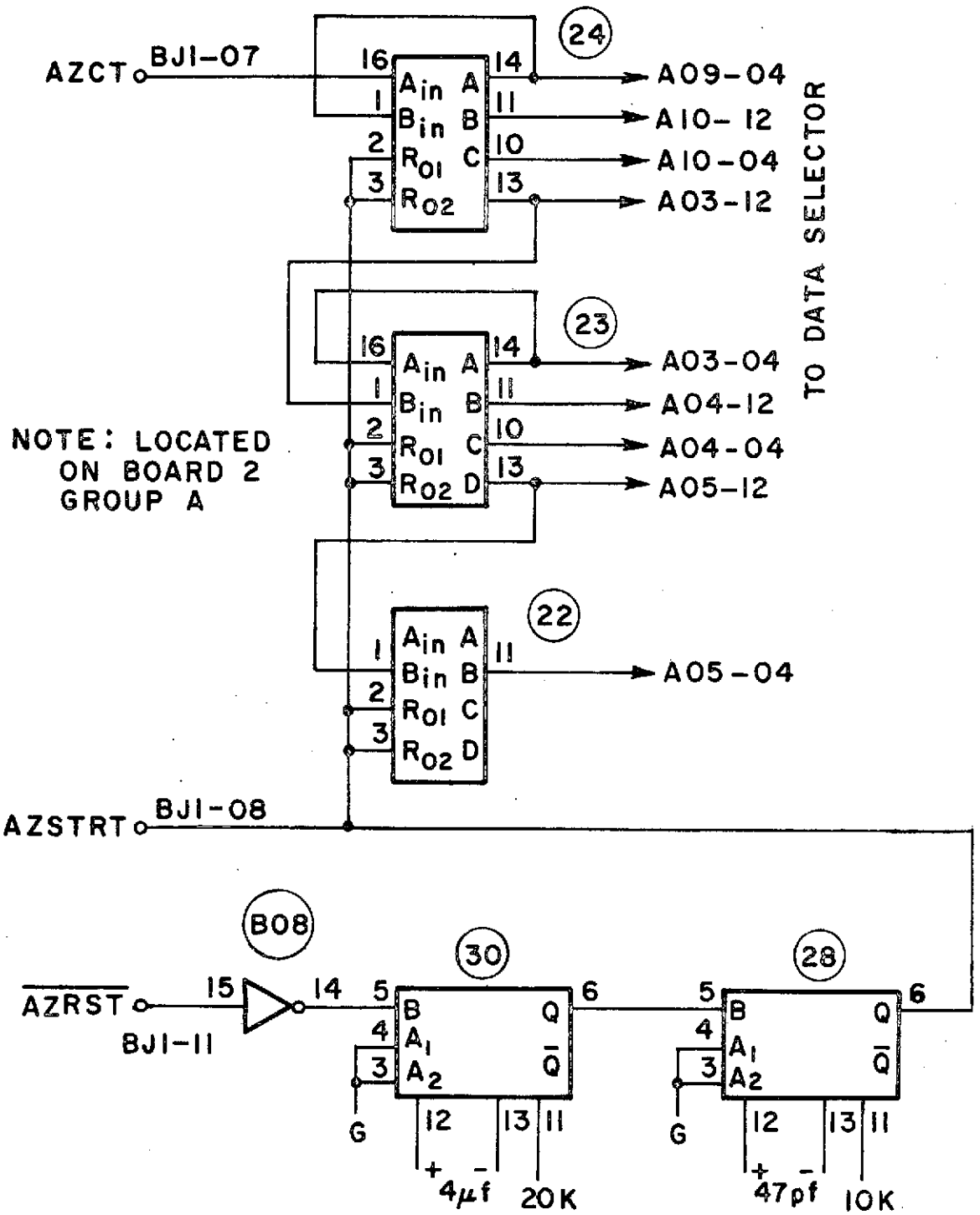


Fig. 22. Azimuth angle counter.

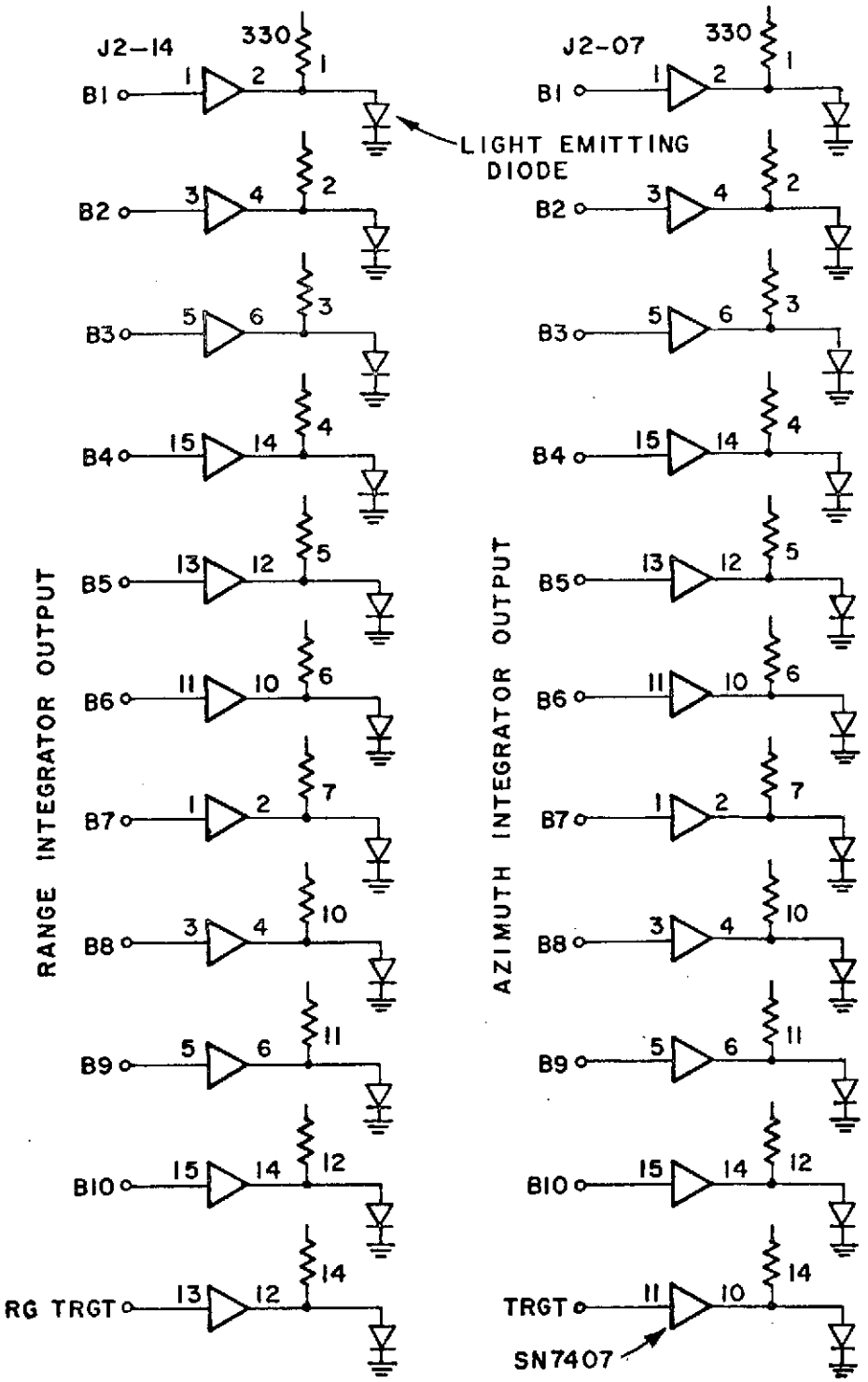


Fig. 23. LED driver 1.

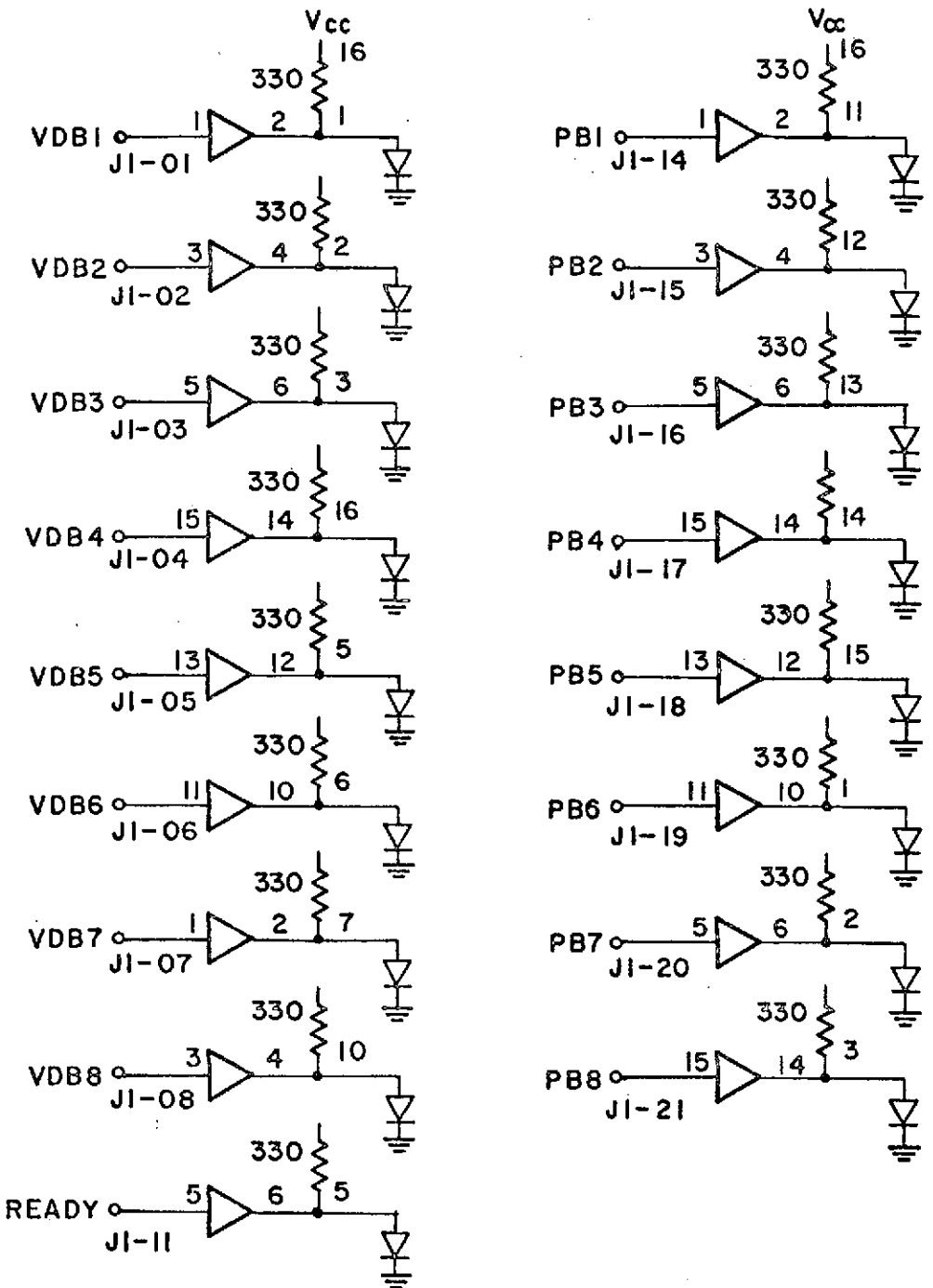


Fig. 24. LED driver 2.

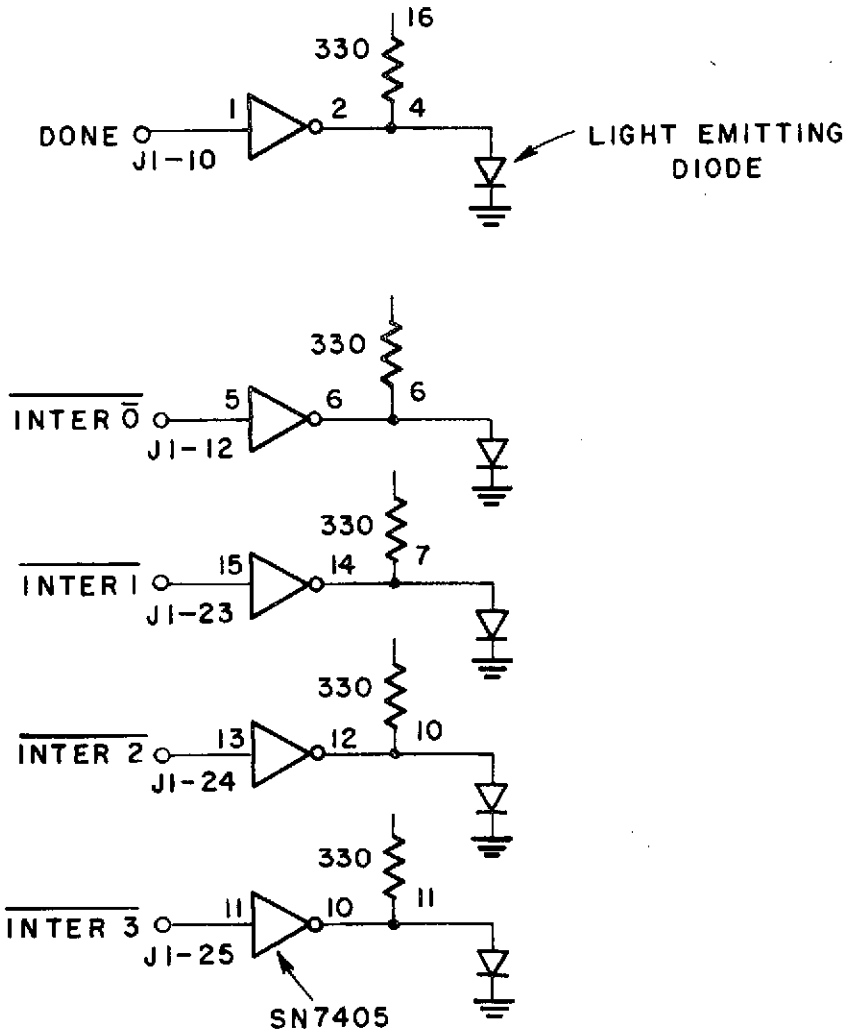


Fig. 25. LED driver 3.

Azimuth Integrator Sum	(10 bits)
Range Integrator Sum	(10 bits)
Azimuth Target Flag	
Range Target Flag	
Video A/D Output	(8 bits)
Power A/D Output	(8 bits)
Interrupts	(4)
Done Signal	
Ready Signal.	

This concludes the circuit diagrams for the low resolution radar digital interface. Proposed modifications to this interface will be discussed in Appendix A. The software for the data acquisition will now be discussed.

III. LOW RESOLUTION SOFTWARE

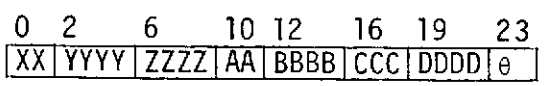
A. Introduction

In this section the programs written to acquire and process the data from the low resolution radar interface are discussed. The data acquisition program written for the SDS 910 is written in SDS 910/920 Assembler. Since a working knowledge of the SDS 910 instruction set is required to fully understand the program, a flow chart will be used to describe its operation. A listing of the program and a detailed flow chart are presented in Appendix C. To process the recorded data, a Fortran IV subroutine was written for the Datacraft 6024 computer. This subroutine converts the recorded data into a form suitable for processing. Its operation will also be described in this section and the listings presented in Appendix C.

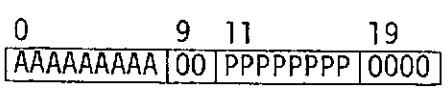
B. SDS 910 Data Acquisition Program

The format of the output data words from the digital interface is determined by the connections made to the data selector. The format of the three data words is shown below.

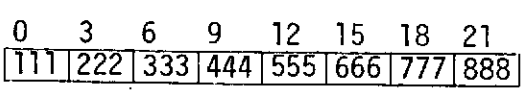
Clock Word



Azimuth-Power Word



Video Data Word



where

XX = BCD hundreds of days digit
YYYY = BCD tens of days digit
ZZZZ = BCD units of days digit

AA = BCD tens of hours digit
BBBB = BCD units of hours digit
CCC = BCD tens of minutes digit
DDDD = BCD units of minutes digit

AAAAAAAA = binary value of azimuth angle of antenna
PPPPPPPP = modified two's complement binary value of transmitted power
111,222,···888 = binary value of video return, 3 bits per range bin

A flow chart for the data acquisition program is shown in Fig. 26. Due to core limitations it is necessary to record several segments of the antenna sweep to get a complete scan on tape. For this reason, the program has two modes. The first, shown in the upper loop, is the data mode. In this mode the program is waiting for the antenna to sweep past the point where the last recorded segment ended. The second mode, shown in the lower loop, is the wait mode. The program enters this mode after a segment has been recorded and is waiting for the antenna to finish its current sweep. The program mode is changed by modifying the instruction which is executed when the priority 3 interrupt is received.

In both of these modes, the program keeps track of the current azimuth angle, AZANGL, and checks it against the last azimuth angle of the previous recorded segment, LASTAZ. The data mode is entered when AZANGL is less than LASTAZ. Data is actually recorded when AZANGL is greater than LASTAZ. This noted by the data flag, FLAG.

Currently, the program writes fifty-seven look angles per record. This results in a record length of 3420 characters. To record a complete scan, five segments are required. If the record length is changed, the program must be changed and the Scan Control Module in the interface must be modified.

C. Fortran IV Routines for Data Processing

After a seven track data tape has been written and converted to nine track, the recorded data must be prepared for processing. As seen earlier the data has been compressed for more efficient storage. Three subroutines were written for the Datacraft 6024 to perform this task. Listings are presented in Appendix C.

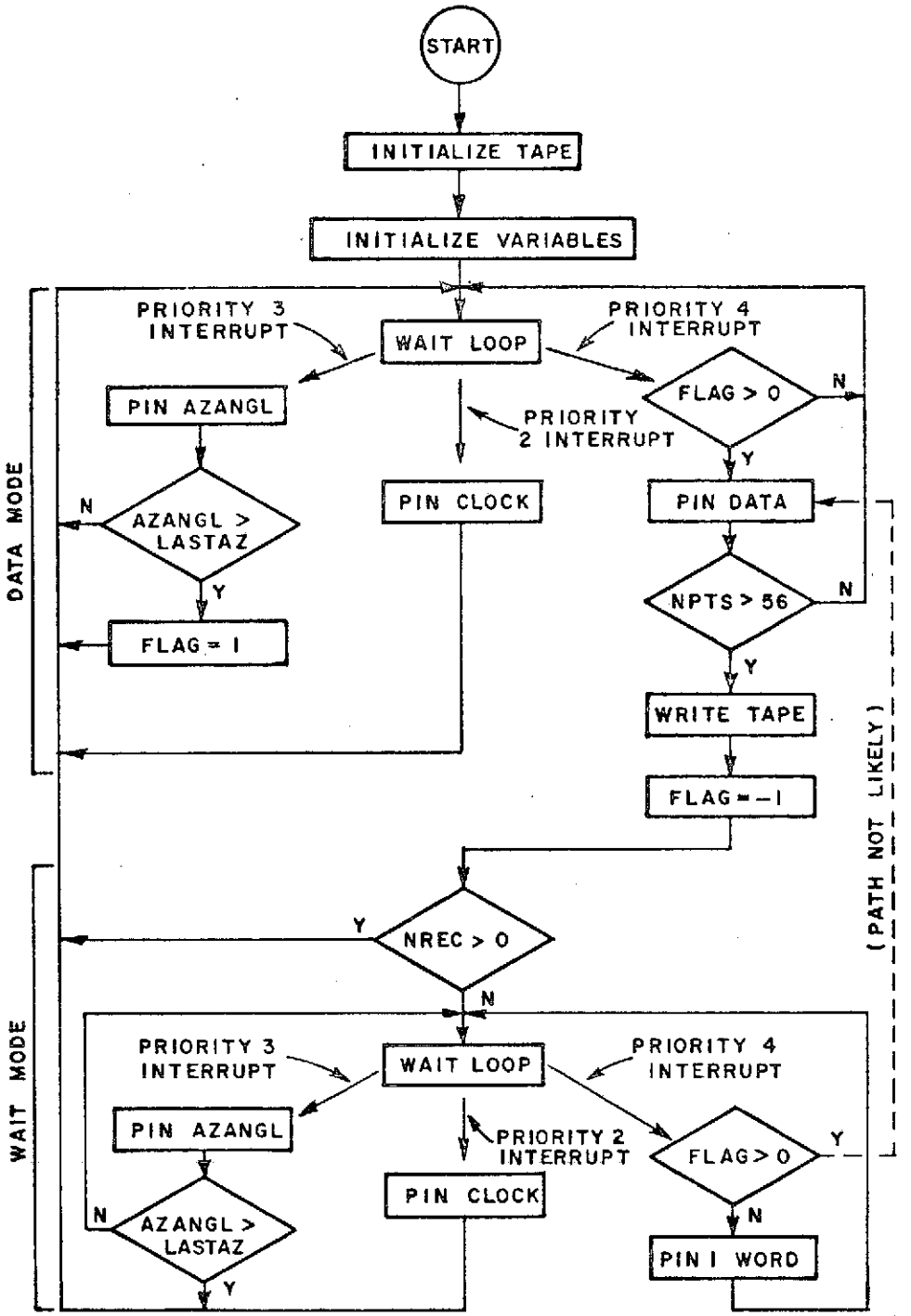


Fig. 26. SDS 910 data acquisition program - simplified flow chart.

The first subroutine DECODE, is called as shown below.

CALL DECODE (IBUF, DAYTIME, ANGLE, RETURN, POWER, ILENTH)

This subroutine uses raw data from the data tape and decodes it into four arrays which give the date, time, azimuth angle, average power and video return for each look angle. The integer variables are DAYTIME, ANGLE, RETURN and POWER, respectively. The raw data is passed to the subroutine in the integer array, IBUF, the length of which is specified by the integer variable, ILENTH.

There are two possible lengths for IBUF. If the raw data is from a nine track tape which has been generated from a seven track tape, the record length will be 1140 of the Datacraft computer's 24 bit word. When the execution of the subroutine is complete, IBUF has been compressed from three characters per 24 bit word to four characters per 24 bit word. This reduces the record length to 855 words. It is suggested for more efficient operation that the nine track tape be recopied to another nine track tape with the 855 word record length. To decode these tapes ILENTH is set to 855.

The outputs from the subroutine are all integer arrays. The DAYTIME array is a linear array 57 elements long. Each element is the Julian date multiplied by 10^4 and the GMT time added together for each look angle. Thus the number 236 1358 is day 236 at 1358 GMT. The ANGLE array is also a linear array, 57 elements long, which contains the integer azimuth angle in degrees for each look angle of the video return. The integer array RETURN is a two dimensional array 57 rows by 100 columns. There is a one to one correspondence to each row in RETURN and each element in DAYTIME, ANGLE and POWER. The number in each element of RETURN is the binary output from the A/D convertor for each range bin. A maximum return of 7 represents 4.375 volts or more. Returns of 4, 2 and 1 represent 2.500, 1.250 and .625 volts respectively. The final output array, POWER, is a measure of the average transmitted power. The power monitor used has an output of 0 to -5 volts. The number in each element of POWER is the absolute value of this voltage in hundreths of a volt. A calibration scale between the output voltage from the power monitor and the actual transmittal power has not been prepared yet. However, the linearity of the power monitor output voltage has been checked to a 6 dB power reduction. That is, a one-fourth power attenuation caused the full power output voltage to drop by one-fourth.

The DECODE subroutine calls two other special purpose subroutines. The first of these is SHFT. This subroutine unpacks the eight 3 bit video return words from a single 24 bit word. Each video return word is stored, right justified, in a full 24 bit word. The unpacked video word is a conventional integer number.

The second subroutine is called PACK, which removes the two blank bits added to each tape character in the seven to nine track conversion. This is done so that the data processed by DECODE corresponds directly to data as it appeared in the SDS 910. Also by removing the blanks the required storage is reduced from 1140 words to 855 words.

This concludes the documentation of the low resolution digital interface system. As explained earlier this report is intended to be a working document and will be changed as the system is updated. The following appendices detail proposed changes, fabrication details and computer program listings.

APPENDIX A
INTEGRATION CONTROL

Figures A-1, A-2 and A-3 show the additional circuitry and the modifications required to incorporate a 32 pulse integration capability, with a 5 ms spacing between pulses.

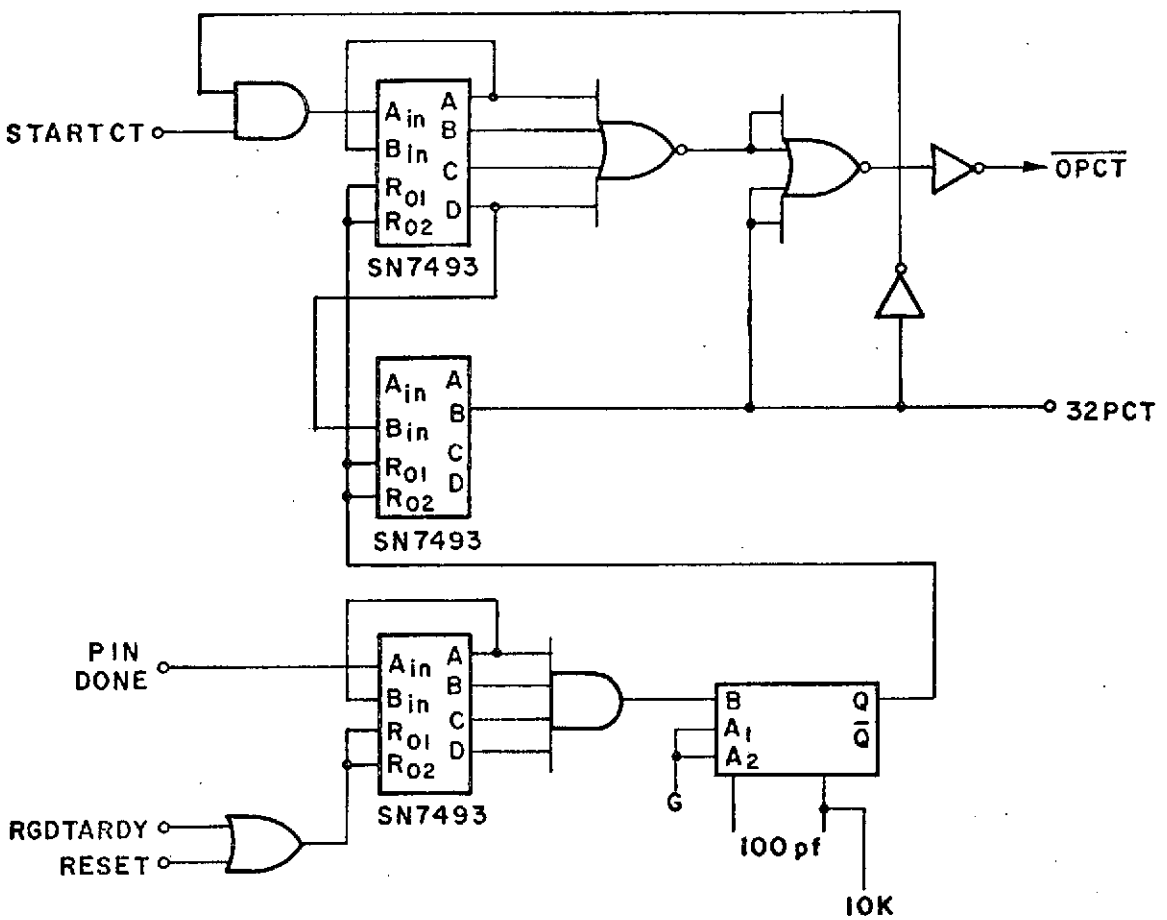


Fig. A-1. Integration control module.

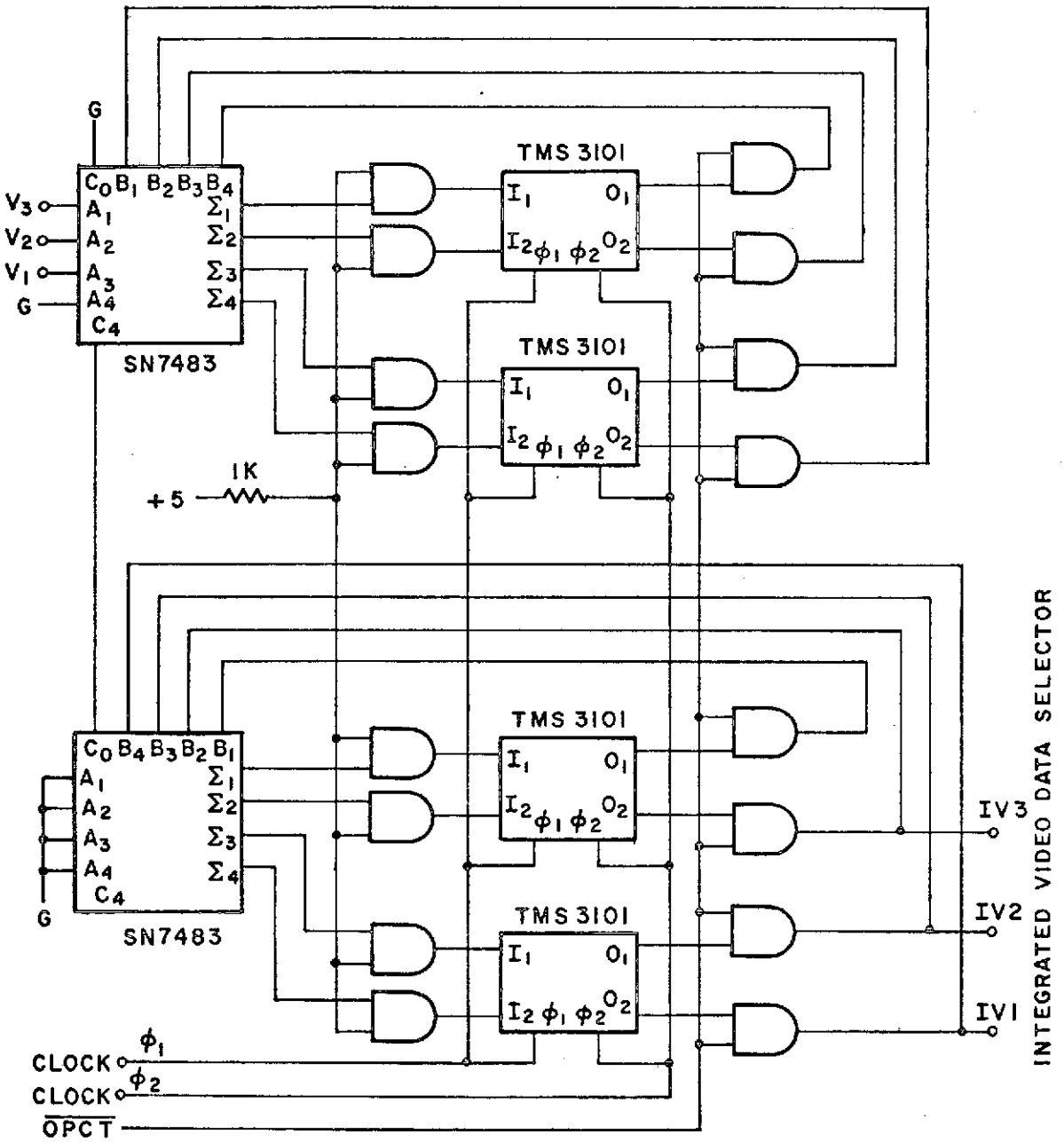


Fig. A-2. Pulse integrator module.

1. Remove wire from 1B05-11, RGTRGT to 1A04-05.
2. Connect 1A04-05 to an I/O header, now labelled 32 PCT.
3. Connect 2B17-06 to an I/O header, now labelled PINDONE.
4. Reconnect cable wire to 1AJ2-02 to V1 on Pulse Integrator.
   Reconnect cable wire to 1AJ2-03 to V2 on Pulse Integrator.
   Reconnect cable wire to 1AJ2-04 to V3 on Pulse Integrator.
5. Remove cable wires to BJ1-04, BJ1-03, BJ1-02.
6. Connect IV3 to BJ1-04, IV2 to BJ1-03, IV1 to BJ1-02.
7. Connect A06-05 to STARTCT on Integrator Control.
8. Connect IBJ2-17, RGDTARDY to RGDTARDY on Integrator Control.
9. Move shift register clock drivers to Pulse Integrator board and reconnect clock signals $\overline{\phi 1}$ and $\overline{\phi 2}$.
10. Remove wire from 1A04-15 to 1A05-13 and reconnect to 1A05-10.

Fig. A-3. Wiring changes needed to install Pulse Integrator.

The Integration Control Module generates the signals which control the integration. The integrator is reset on a zero pulse count. Each STARTCT signal increments the two counters until a count of 32 is reached. At this point, the counter input is disabled and the 32 PCT signal allows the RGDTARDY signal in the A/D Control Module to go high through 1A04-05. The bottom counter in Fig. A-1 counts the number of times the computer reads data from the interface signaled by PINDONE from the Interrupt Control Module. After fifteen parallel input operations, the pulse counters are reset and the next look angle is digitized.

The Pulse Integrator Module uses an 800 bit shift register memory to perform the digital integration. The partial sum for each range bin is stored segmentally in the shift register and recirculated through the adder for each radar pulse. Since the number of pulses integrated is an integer power of two, the average is obtained by looking at only the three highest order bits.

These modifications are based on the assumption that the sweep rate of the antenna has been slowed down so that the look angle change during the integration period is small. This will require the Azimuth Angle Counter and the Azimuth Angle Buffer Modules to be modified.

APPENDIX B
CABLE CONNECTIONS

This appendix contains fabrication details of the low resolution radar digital interface. The IC type numbers and their locations are also shown here. Tables showing the cable interconnections are presented along with a list of abbreviations. The power supply wire color codes are also presented.

TABLE B-1
A/D BOARD CABLES

FROM A/D	TO BOARD	LABEL	FROM	TO	LABEL
J1-01	2B25-01	B1MSB PWR	J2-01	LEDJ1-14	POWER A/D
J1-02	2B25-02	B2 PWR	J2-02	LEDJ1-15	POWER A/D
J1-03	2B25-03	B3 PWR	J2-03	LEDJ1-16	POWER A/D
J1-04	2B25-04	B4 PWR	J2-04	LEDJ1-17	POWER A/D
J1-05	2B25-05	B5 PWR	J2-05	LEDJ1-18	POWER A/D
J1-06	2B25-15	B6 PWR	J2-06	LEDJ1-19	POWER A/D
J1-07	2B25-14	B7 PWR	J2-07	LEDJ1-20	POWER A/D
J1-08	2B25-13	B8LSBPWR	J2-08	LEDJ1-21	POWER A/D
J1-09	2B25-06	PWRADSTRT	J2-09		
J1-10			J2-10		
J1-11			J2-11		
J1-12			J2-12		
J1-13	2B25-07	GND	J2-13		GND
J1-14	1AJ2-02	B1MSBVIDEO	J2-14	LEDJ1-01	VIDEO A/D
J1-15	1AJ2-03	B2 VIDEO	J2-15	LEDJ1-02	VIDEO A/D
J1-16	1AJ2-04	B3 VIDEO	J2-16	LEDJ1-03	VIDEO A/D
J1-17		B4 VIDEO	J2-17	LEDJ1-04	VIDEO A/D
J1-18		B5 VIDEO	J2-18	LEDJ1-05	VIDEO A/D
J1-19		B6 VIDEO	J2-19	LEDJ1-06	VIDEO A/D
J1-20		B7 VIDEO	J2-20	LEDJ1-07	VIDEO A/D
J1-21		B8 VIDEO	J2-21	LEDJ1-08	VIDEO A/D
J1-22	1AJ2-01	ADSTRT	J2-22		
J1-23	1AJ2-12	ADCLCK	J2-23		
J1-24			J2-24		
J1-25			J2-25		
J1-26		GND	J2-26		GND

TABLE B-2
CABLES FOR BOARD 1 GROUP A

FROM	TO	LABEL
1AJ1-01	B2J1-09	1 μs CLK
1AJ1-02	CLP-24	1 ms CLK
1AJ1-03	RI	FIRE
1AJ1-04	RI	AZRESET
1AJ1-05	CLP-01	CLKUMB1
1AJ1-06	CLP-02	CLKUMB2
1AJ1-07	CLP-03	CLKUMB4
1AJ1-08	CLP-04	CLKUMB8

FROM	TO	LABEL
1AJ2-01	ADJ1-22	ADSTRT
1AJ2-02	ADJ1-14	VB1
1AJ2-03	ADJ1-15	VB2
1AJ2-04	ADJ1-16	VB3
1AJ2-05		
1AJ2-06		
1AJ2-07		
1AJ2-08		
1AJ2-09		
1AJ2-10		
1AJ2-11		
1AJ2-12	ADJ1-23	ADCLK

TABLE B-3
CABLES FOR BOARD 1 GROUP B

FROM	TO	LABEL
1BJ1-01	LEDJ2-01	AZ INTEG
1BJ1-02	LEDJ2-02	AZ INTEG
1BJ1-03	LEDJ2-03	AZ INTEG
1BJ1-04	LEDJ2-04	AZ INTEG
1BJ1-05	LEDJ2-05	AZ INTEG
1BJ1-06	LEDJ2-06	AZ INTEG
1BJ1-07	LEDJ2-07	AZ INTEG
1BJ1-08	LEDJ2-08	AZ INTEG
1BJ1-09	LEDJ2-09	AZ INTEG
1BJ1-10	LEDJ2-10	AZ INTEG
1BJ1-11	LEDJ2-11	RGTRGT
1BJ1-12	LEDJ2-12	TRGTFLG
1BJ1-13	LEDJ2-13	GND
1BJ1-14	LEDJ2-14	RG INTEG
1BJ1-15	LEDJ2-15	RG INTEG
1BJ1-16	LEDJ2-16	RG INTEG
1BJ1-17	LEDJ2-17	RG INTEG
1BJ1-18	LEDJ2-18	RG INTEG
1BJ1-19	LEDJ2-19	RG INTEG
1BJ1-20	LEDJ2-20	RG INTEG
1BJ1-21	LEDJ2-21	RG INTEG
1BJ1-22	LEDJ2-22	RG INTEG
1BJ1-23	LEDJ2-23	RG INTEG
1BJ1-24		
1BJ1-25		
1BJ1-26	LEDJ2-26	GND

FROM	TO	LABEL
1BJ2-01		
1BJ2-02		
1BJ2-03		
1BJ2-04		
1BJ2-05		
1BJ2-06		
1BJ2-07		
1BJ2-08		
1BJ2-09		
1BJ2-10		
1BJ2-11		
1BJ2-12	REAR PANEL	-12 VOLTS
1BJ2-13		GND
1BJ2-14	2BJ1-02	DB1MSB
1BJ2-15	2BJ1-03	DB2
1BJ2-16	2BJ1-04	DB3
1BJ2-17	2BJ1-05	RGDTARDY
1BJ2-18	2BJ1-01	RGTRGT
1BJ2-19		RGTRGT
1BJ2-20	2BJ1-10	PWRAD
1BJ2-21	2BJ1-06	SHFTFMTR
1BJ2-22		
1BJ2-23		
1BJ2-24		
1BJ2-25		
1BJ2-26		

TABLE B-4
CABLES FOR BOARD 2 GROUP A

FROM	TO	LABEL
2AJ1-01	CLP-01	CLKUM1
2AJ1-02	CLP-02	CLKUM2
2AJ1-03	CLP-03	CLKUM4
2AJ1-04	CLP-04	CLKUM8
2AJ1-05	CLP-05	CLKTM1
2AJ1-06	CLP-06	CLKTM2
2AJ1-07	CLP-07	CLKTM4
2AJ1-08		
2AJ1-09	CLP-08	CLKUH1
2AJ1-10	CLP-09	CLKUH2
2AJ1-11	CLP-10	CLKUH4
2AJ1-12	CLP-11	CLKUH8
2AJ1-13		GND
2AJ1-14	CLP-12	CLKTH1
2AJ1-15	CLP-13	CLKTH2
2AJ1-16	CLP-14	CLKUD1
2AJ1-17	CLP-15	CLKUD2
2AJ1-18	CLP-16	CLKUD4
2AJ1-19	CLP-17	CLKUD8
2AJ1-20	CLP-18	CLKTD1
2AJ1-21	CLP-19	CLKTD2
2AJ1-22	CLP-20	CLKTD4
2AJ1-23	CLP-21	CLKTD8
2AJ1-24	CLP-22	CLKHD1
2AJ1-25	CLP-23	CLKHD2
2AJ1-26		GND

FROM	TO	LABEL
2AJ2-01	CP-01	PIN BOMSB
2AJ2-02	CP-02	PIN B1
2AJ2-03	CP-03	PIN B2
2AJ2-04	CP-04	PIN B3
2AJ2-05	CP-05	PIN B4
2AJ2-06	CP-06	PIN B5
2AJ2-07	CP-07	PIN B6
2AJ2-08	CP-08	PIN B7
2AJ2-09	CP-09	PIN B8
2AJ2-10	CP-10	PIN B9
2AJ2-11	CP-11	PIN B10
2AJ2-12	CP-12	PIN B11
2AJ2-13		GND
2AJ2-14	CP-13	PIN B12
2AJ2-15	CP-14	PIN B13
2AJ2-16	CP-15	PIN B14
2AJ2-17	CP-16	PIN B15
2AJ2-18	CP-17	PIN B16
2AJ2-19	CP-18	PIN B17
2AJ2-20	CP-19	PIN B18
2AJ2-21	CP-20	PIN B19
2AJ2-22	CP-21	PIN B20
2AJ2-23	CP-22	PIN B21
2AJ2-24	CP-23	PIN B22
2AJ2-25	CP-24	PIN B23
2AJ2-26	CP-36	GND

TABLE B-5
CABLES FOR BOARD 2 GROUP B

FROM	TO	LABEL	FROM	TO	LABEL
2BJ1-01	1BJ2-19	$\overline{\text{RGTRGT}}$	2BJ2-01	CP-32	$\overline{\text{DONE}}$
2BJ1-02	1BJ2-14	DB1MSB	2BJ2-02	CP-34	READY
2BJ1-03	1BJ2-15	DB2	2BJ2-03	IP-01	INTER1
2BJ1-04	1BJ2-16	DB3	2BJ2-04	IP-02	INTER2
2BJ1-05	1BJ2-17	RGDTARDY	2BJ2-05	IP-03	INTER3
2BJ1-06		SHIFTFMTR	2BJ2-06	IP-04	INTER4
2BJ1-07	KH BUFFER	AZIN	2BJ2-07		
2BJ1-08	1AJ1-04	AZRESET	2BJ2-08		
2BJ1-09	1AJ1-01	1μSCLK	2BJ2-09		
2BJ1-10	1BJ2-20	PWRAD	2BJ2-10		
2BJ1-11	KH BUFFER	$\overline{\text{AZRESET}}$	2BJ2-11		
2BJ1-12			2BJ2-12	IP-12	+8
2BJ1-13		GND	2BJ2-13	IP-14	GND
2BJ1-14	FP-S1	HALT	2BJ2-14		
2BJ1-15	FP-S2	RESET INTER	2BJ2-15		
2BJ1-16	LEDJ1-10	DONE	2BJ2-16		
2BJ1-17	LEDJ1-11	READY	2BJ2-17		
2BJ1-18	LEDJ1-12	INTER1	2BJ2-18		
2BJ1-19	LEDJ1-13	INTER2	2BJ2-19		
2BJ1-20	LEDJ1-14	INTER3	2BJ2-20		
2BJ1-21	LEDJ1-15	INTER4	2BJ2-21		
2BJ1-22			2BJ2-22		
2BJ1-23			2BJ2-23		
2BJ1-24			2BJ2-24		
2BJ1-25			2BJ2-25		
2BJ1-26			2BJ2-26	REAR PANEL 1μS SINE	

TABLE B-6
POWER SUPPLY WIRING COLOR CODES

COLOR	VOLTAGE	CURRENT CAPABILITIES
White	115v AC	
Black	115v AC	
Green	Ground	
Red	+5v DC	9 A
Gray	+12v DC	400 mA
Blue	-12v DC	400 mA
Brown	+15v DC	100 mA
Orange	-15v DC	100 mA

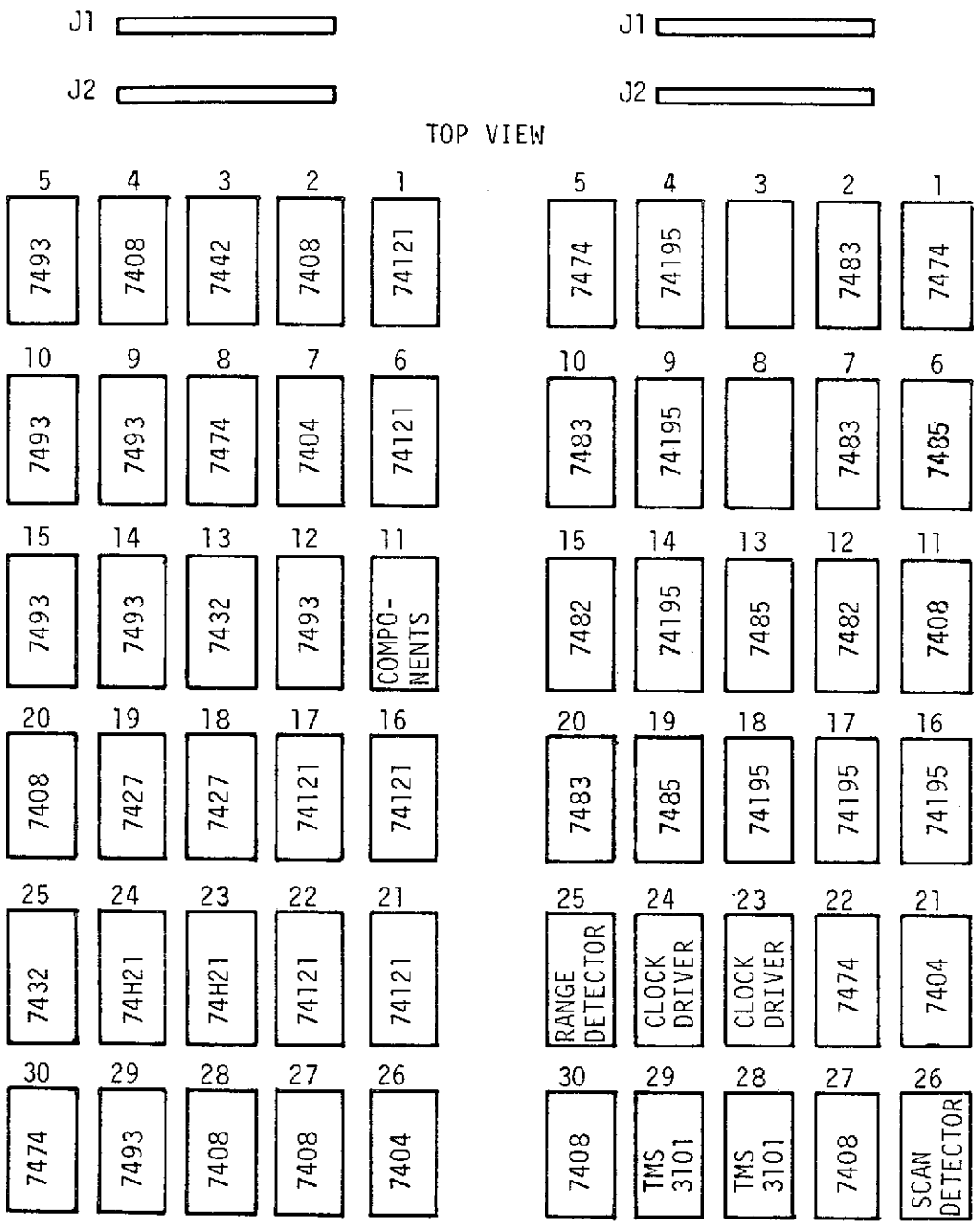


Fig. B-1. IC locations for Board 1.

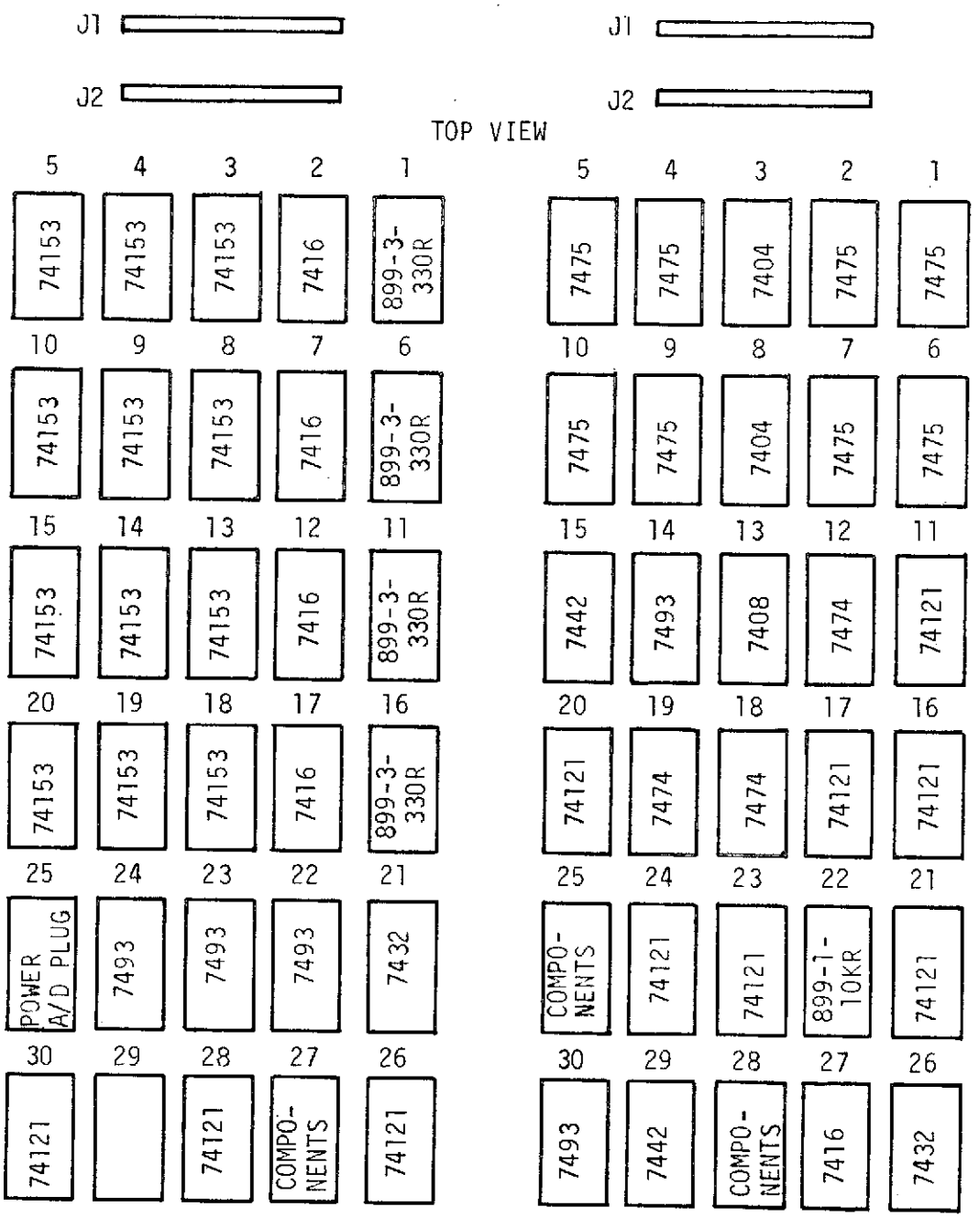


Fig. B-2. IC locations for Board 2.

APPENDIX C
DATA ACQUISITION PROGRAM

The listing for the SDS 910 data acquisition program and a detailed flow chart are presented in this appendix. Also presented are listings for the Fortran IV data processing subroutines.

```
*
* LOW RESOLUTION RADAR DATA ACQUISITION PROGRAM
* RECORDS DATA ON MAG TAPE UNIT 1
* 57 LOOK ANGLES PER RECORD  855 WORDS PER RECORD
* VERSION 2-D 16 JANUARY 1973
*
* SET UP INTERRUPT LOCATION INSTRUCTIONS
*
            0031            ORG     31
0031  0 43 00100             BRM     END             END OF WORD INTERRUPT
            0033            ORG     33
0033  0 43 00100             BRM     END             END OF RECORD INTERRUPT
            0100            ORG     100
0100  0 00 00000    END     PZE
*
            0200            ORG     200
*
* PRIORITY INTERRUPT LOCATIONS
*
0200  0 43 00316             BRM     ABORT           ABORT INTERRUPT
0201  0 43 00335             BRM     CLOCK           CLOCK INTERRUPT
0202  0 43 00341    S202     BRM     AZI             AZIMUTH INTERRUPT
0203  0 43 00405             BRM     DATAIN          VIDEO DATA INTERRUPT
*
* START OF ACQUISTION PROGRAM
* PREPARE DATA TAPE LEADER
*
0204  0 00 00000    START    HLT
0205  0 40 20400             BPT     1               TEST BREAKPOINT 1
0206  0 01 00205             BRU     *-1             IF SET GO BACK AND WAIT
0207  0 40 12011             BIT     1               TEST FOR TAPE AT LOAD POINT
0210  0 01 00212             BRU     *+2             YES, CONTINUE
0211  0 01 00224             BRU     S20             NO, WRITE LEADER
0212  0 43 00425             BRM     READY           TEST FOR TAPE READY
0213  0 40 14011             FPT     1               TEST FOR FILE PROTECT RING
0214  0 01 00213             BRU     *-1             FILE PROTECTED SO WAIT
0215  0 02 03671             ETF     1,4             ERASE TAPE FORWARD
0216  0 71 00441             LDX     ND200           LOAD COUNT TO ERASE 4 INCHES
0217  0 12 00461             MIW     ZERO            WRITE A ZERO
0220  0 41 00217             BRX     *-1             CONTINUE LOOP
0221  0 02 14000             TOP
0222  0 46 30003    S21      CLR
0223  0 35 00456             STA     NREC            NUMBER OF RECORDS SET TO ZERO
0224  0 43 00271    S20      BRM     INIT            INITIALIZE VARIABLES
*
* INTERRUPT WAIT LOOP
*
0225  0 02 20002    WAIT     EIR                     ENABLE INTERRUPTS
0226  0 40 20400             BPT     1               TEST BREAKPOINT 1 FOR AN ABORT
0227  0 01 00231             BRU     *+2             BRANCH TO ABORT CALL
0230  0 01 00226             BRU     *-2             BREAKPOINT NOT SET SO IDLE
0231  0 02 20004             DIR                     DISABLE INTERRUPTS
0232  0 01 00317             BRU     ABORT+1         BRANCH TO ABORT ROUTINE
*
* WRITE DATA ON TAPE
*
0233  0 02 20004    M20      DIR                     DISABLE INTERRUPTS
0234  0 43 00425             BRM     READY           TEST TAPE READY
0235  0 71 00443             LDX     ND855           LOAD WORD COUNT
0236  0 02 03651             WTB     1,4             TAPE UNIT 1, WRITE BINARY MODE
0237  2 12 02211             MIW     IOBUFF+855,2
```

Fig. C-1. SDS 910 data acquisition program.

```
0240  0 41 00237           BRX     *-1
0241  0 02 14000           TOP                     TERMINATE OUTPUT
*
* RESET VARIABLES FOR NEXT RECORD
*       0  0
0242  0 76 02173           LDA     IOBUFF+841      GET LAST AZIMUTH ANGLE
0243  0 66 00017           RSH     15              ALIGN FOR CONVERSION TO NUMBER
0244  0 35 00447           STA     LASTAZ          SAVE FOR MASKING OPERATION
0245  0 76 00436           LDA     MSK             LOAD MASK
0246  0 14 00447           ETR     LASTAZ          MASK AZIMUTH ANGLE INTO A
0247  0 35 00447           STA     LASTAZ          STORE AZIMUTH ANGLE
0250  0 46 30003           CLR
0251  0 35 00452           STA     NPTS            LOOK ANGLE COUNT SET TO ZERO
0252  0 77 00462           EAX     IOBUFF          GET ADDRESS OF I/O BUFFER
0253  0 37 00460           STX     INPNT           STORE DATA INPUT POINTER
0254  0 76 00434           LDA     FLGRST          RESET FLAG FOR DATA INPUT
0255  0 35 00450           STA     FLAG            STORE
0256  0 76 00455           LDA     AZINT2          GET AZIMUTH INTERRUPT ROUTINE
0257  0 35 00202           STA     S202            STORE IN AZ INTERRUPT LOC
0260  0 46 30003           CLR
0261  0 71 00443           LDX     ND855           GET BUFFER COUNT
0262  2 35 02211           STA     IOBUFF+855,2    CLEAR INPUT BUFFER
0263  0 41 00262           BRX     *-1             CONTINUE LOOP
0264  0 61 00456           MIN     NREC            INCREMENT RECORD COUNT
0265  0 61 00457           MIN     NREC1           INCREMENT SCAN COUNT
*
* TEST FOR PROGRAM MODE CHANGE
*
0266  0 53 00457           SKN     NREC1           TEST FOR POSITIVE
0267  0 01 00224           BRU     S20             POSITIVE,SO SCAN RECORDED
0270  0 01 00225           BRU     WAIT            SCAN NOT COMPLETE, GET MORE DATA
*
* SUBROUTINES
*
0271  0 00 00000    INIT   PZE
0272  0 77 00462           EAX     IOBUFF          GET ADDRESS OF I/O BUFFER
0273  0 37 00460           STX     INPNT           STORE IN DATA POINTER
0274  0 76 00444           LDA     NOSCAN          GET SCAN COUNT
0275  0 35 00457           STA     NREC1           STORE IN SCAN COUNTER
0276  0 46 30003           CLR
0277  0 35 00452           STA     NPTS            ZERO LOOK ANGLE COUNT
0300  0 35 00447           STA     LASTAZ          SET LAST AZ ANGLE TO ZERO
0301  0 76 00434           LDA     FLGRST          RESET FLAG FOR DATA INPUT
0302  0 35 00450           STA     FLAG            STORE IN FLAG
0303  0 77 00341           EAX     AZ1             GET AZ INTERRUPT ROUTINE ADDRS
0304  0 37 00453           STX     TMP             SAVE IN TEMP STORAGE
0305  0 76 00433           LDA     BRMINS          GET BRM OPCODE
0306  0 55 00453           ADD     TMP             ADD LOCATION
0307  0 35 00454           STA     AZINT1          STORE INSTRUCTION
0310  0 77 00364           EAX     AZ2             GET AZ2 ADDRESS
0311  0 37 00453           STX     TMP             SAVE IN TEMP STORAGE
0312  0 76 00433           LDA     BRMINS          GET BRM OPCODE
0313  0 55 00453           ADD     TMP             ADD ADDRESS
0314  0 35 00455           STA     AZINT2          STORE
0315  0 51 00271           BRR     INIT            RETURN
*
0316  0 00 00000    ABORT  PZE
0317  0 02 20004           DIR                     DISABLE INTERRUPTS
0320  0 02 14000           TOP                     STOP TAPE IF RUNNING
0321  0 43 00425    EOFT   BRM     READY           TEST TAPE READY
```

Fig. C-1. (Contd).

```
0322  0 71 00442          LDX     ND150          LOAD COUNT FOR EOF RECORD
0323  0 02 03671          ETF     1,4            ERASE TAPE
0324  0 12 00461          MIW     ZERO           WRITE ZEROS
0325  0 41 00324          BRX     *-1            CONTINUE LOOP
0326  0 02 14000          TOP                    STOP TAPE
0327  0 43 00425          BRM     READY          TEST TAPE READY
0330  0 02 02051          WTD     1,1            START TAPE FOR EOF
0331  0 12 00437          MIW     EOF            WRITE EOF MARK
0332  0 02 14000          TOP                    TERMINATE OUTPUT
0333  0 76 00456          LDA     NREC           NUMBER OF RECORDS IN A
0334  0 01 00204          BRU     START          RETURN TO START OF PROGRAM
*
0335  0 00 00000  CLOCK    PZE
0336  0 33 40460          PIN*    INPNT          GET CLOCK DATA FROM INTERFACE
0337  0 61 00460          MIN     INPNT          INCREMENT ADDRESS POINTER
0340  0 01 40335          BRU*    CLOCK          CLEAR INTERRUPT AND RETURN
*
0341  0 00 00000  AZ1      PZE
0342  0 33 40460          PIN*    INPNT          GET AZIMUTH ANGLE FROM INTERFACE
0343  0 76 40460          LDA*    INPNT          LOAD ANGLE FOR TEST
0344  0 53 00450          SKN     FLAG           TEST DATA FLAG
0345  0 01 00356          BRU     A15            FLAG POSITIVE, TEST AZ ANGLE
0346  0 66 00017  A05      RSH     15             ALIGN AZ ANGLE WORD
0347  0 35 00446          STA     AZANGL         SAVE FOR MASK
0350  0 76 00436          LDA     MSK
0351  0 14 00446          ETR     AZANGL         MASK AZIMUTH ANGLE
0352  0 73 00447          SKG     LASTAZ         SKIP IF GREATER THAN LAST AZ
0353  0 01 00360          BRU     A10            NOT GREATER SO WAIT FOR NEXT AZ
0354  0 76 00435          LDA     FLGSET         AZ GREATER SO SET FLAG
0355  0 35 00450          STA     FLAG           STORE FLAG
0356  0 61 00460  A15      MIN     INPNT          INCREMENT POINTER
0357  0 01 40341          BRU*    AZ1            CLEAR INTERRUPT AND RETURN
0360  0 60 00460  A10      MDE     INPNT          NOT DATA SO DECREMENT POINTER
0361  0 76 00434          LDA     FLGRST         RESET FLAG
0362  0 35 00450          STA     FLAG           STORE FLAG
0363  0 01 40341          BRU*    AZ1            CLEAR INTERRUPT AND RETURN
*
0364  0 00 00000  AZ2      PZE
0365  0 33 40460          PIN*    INPNT          GET AZIMUTH DATA FORM INTERFACE
0366  0 76 40460          LDA*    INPNT          LOAD INTO A REGISTER
0367  0 66 00017          RSH     15             ALIGN WORD
0370  0 35 00446          STA     AZANGL         SAVE FOR MASK
0371  0 76 00436          LDA     MSK            LOAD MASK
0372  0 14 00446          ETR     AZANGL         MASK AZIMUTH ANGLE
0373  0 73 00447          SKG     LASTAZ         SKIP IF ANGLE GREATER THAN LAST
0374  0 01 00377          BRU     A20            NOT GREATER SO BRANCH TO IDLE
0375  0 60 00460          MDE     INPNT          DECREMENT POINTER
0376  0 01 40364          BRU*    AZ2            CLEAR INTERRUPT AND RETURN
0377  0 76 00454  A20      LDA     AZINT1         SET UP FOR DATA WAIT
0400  0 35 00202          STA     S202           STORE WAIT ROUTINE IN INTER LOC
0401  0 60 00460          MDE     INPNT          RESTORE POINTER
0402  0 76 00434          LDA     FLGRST         RESET FLAG
0403  0 35 00450          STA     FLAG           STORE FLAG
0404  0 01 40364          BRU*    AZ2            CLEAR INTERRUPT AND RETURN
*
0405  0 00 00000  DATAIN   PZE
0406  0 53 00450          SKN     FLAG           SKIP IF FLAG NEGATIVE
0407  0 01 00412          BRU     DATA           FLAG POSITIVE, DATA MODE
0410  0 33 00451  IDLE     PIN     DUMMY          GET ONE WORD FROM INTERFACE
0411  0 01 40405          BRU*    DATAIN         CLEAR INTERRUPT AND RETURN
```

Fig. C-1. (Contd).

```
0412  0 71 00440     DATA   LDX     ND13            GET VIDEO DATA WORD COUNT
0413  0 33 40460            PIN*    INPNT           GET VIDEO DATA FROM INTERFACE
0414  0 61 00460            MIN     INPNT           INCREMENT ADDRESS POINTER
0415  0 41 00413            BRX     *-2             CONTINUE LOOP
0416  0 61 00452            MIN     NPTS            INCREMENT NUMBER OF LOOK ANGLES
0417  0 76 00452            LDA     NPTS            LOAD NPTS INTO A
0420  0 73 00445            SKG     D56             SKIP FOR 57 LOOK ANGLES
0421  0 01 40405            BRU*    DATAIN          CLEAR INTERRUPT AND RETURN
0422  0 77 00233            EAX     M20             GET ADDRESS OF TAPE WRITE
0423  0 37 00405            STX     DATAIN          STORE AS RETURN ADDRESS
0424  0 01 40405            BRU*    DATAIN          CLEAR INTERRUPT AND RETURN
*
0425  0 00 00000     READY  PZE
0426  0 40 21000            BRT
0427  0 40 10411            TRT     1               TEST TAPE READY
0430  0 01 00432            BRU     *+2             READY SO RETURN
0431  0 01 00427            BRU     *-2             NOT READY SO W*IT
0432  0 51 00425            BRR     READY
*
0433  0 43 00000     BRMINS BRM     0               BRM INSTRUCTION
*
* CONSTANTS
*
0434     77777777  FLGRST DEC     -1
0435     00000001  FLGSET DEC     1
0436     00000777  MSK    OCT     777
0437     17170000  EOF    OCT     17170000
0440     77777763  ND13   DEC     -13
0441     77777470  ND200  DEC     -200
0442     77777552  ND150  DEC     -150
0443     77776251  ND855  DEC     -855
0444     77777773  NDSCAN DEC     -5
0445     00000070  D56    DEC     56
*
* VARIABLES
*
0446  0 00 00000     AZANGL PZE
0447  0 00 00000     LASTAZ PZE
0450  0 00 00000     FLAG   PZE
0451  0 00 00000     DUMMY  PZE
0452  0 00 00000     NPTS   PZE
0453  0 00 00000     TMP    PZE
0454  0 00 00000     AZINT1 PZE
0455  0 00 00000     AZINT2 PZE
0456  0 00 00000     NREC   PZE
0457  0 00 00000     NREC1  PZE
0460  0 00 00000     INPNT  PZE
0461  0 00 00000     ZERO   PZE
*
* INPUT OUTPUT BUFFER
*
0462        1527     IOBUFF BSS     855
2211  0 00 00000     BUFEND PZE
*
* UTILITY ROUTINE TO READ THE DATA TAPE ON THE SDS 910
*          0
2212  0 71 00443            LDX     ND855
2213  0 02 03611            RTB     1,4
2214  2 32 02211            WIM     IOBUFF+855,2
2215  0 41 02214            BRX     *-1
2216  0 00 00000            HLT
2217  0 01 00462            BRU     IOBUFF
           0000             END
           0000     ERRORS 1
```

Fig. C-1. (Contd).

```
      SUBROUTINE PACK(II1,II2,II3,II4,IO)
C
C THIS SUBROUTINE REMOVES THE TWO BLANK CHARACTERS PACKED INTO 7 TRACK
C CHARACTERS IN A 7 TO 9 TRACK CONVERSION AND PACKS THE CHARACTERS
C 4 CHARACTERS PER WORD
C II1,II2,II3,II4= FOUR CONSECUTIVE INTEGER WORDS OF UNPACKED DATA
C IO= INTEGER ARRAY OF THREE PACKED WORDS, 4 CHARACTERS PER WORD
C
      DIMENSION IO(3)
       I1=(II1.SHIFT.2).AND.'77000000
      I2=(II1.SHIFT.4).AND.'00770000
      I3=(II1.SHIFT.6).AND.'00007700
      I4=(II2.SHIFT.2).AND.'77000000
      I5=(II2.SHIFT.4).AND.'00770000
      I6=(II2.SHIFT.6).AND.'00007700
      I7=(II3.SHIFT.2).AND.'77000000
      I8=(II3.SHIFT.4).AND.'00770000
      I9=(II3.SHIFT.6).AND.'00007700
      I10=(II4.SHIFT.2).AND.'77000000
      I11=(II4.SHIFT.4).AND.'00770000
      I12=(II4.SHIFT.6).AND.'00007700
      I4=I4.SHIFT.-18
      I5=I5.SHIFT.6
      I6=I6.SHIFT.6
      I7=I7.SHIFT.-12
      I8=I8.SHIFT.-12
      I9=I9.SHIFT.12
      I10=I10.SHIFT.-2
      I11=I11.SHIFT.-2
      IO(1)=I1.OR.I2.OR.I3.OR.I4
      IO(2)=I5.OR.I6.OR.I7.OR.I8
      IO(3)=I9.OR.I10.OR.I11.OR.I12
      RETURN
      END


      SUBROUTINE SHFT(INWRD,OUTWRD)
C
C THIS SUBROUTINE IS USED TO UNPACK THE 3 BIT VIDEO DATA WORDS INTO
C EIGHT 24 BIT INTEGERS
C INWRD= INTEGER INPUT WORD
C OUTWRD= INTEGER ARRAY OF EIGHT 3 BIT WORDS FROM INWRD
C
      INTEGER OUTWRD(8)
      OUTWRD(1)=(INWRD.SHIFT.-21).AND.'7
      OUTWRD(2)=(INWRD.SHIFT.-15).AND.'7
      OUTWRD(3)=(INWRD.SHIFT.-15).AND.'7
      OUTWRD(4)=(INWRD.SHIFT.-12).AND.'7
      OUTWRD(5)=(INWRD.SHIFT.-09).AND.'7
      OUTWRD(6)=(INWRD.SHIFT.-06).AND.'7
      OUTWRD(7)=(INWRD.SHIFT.-03).AND.'7
      OUTWRD(8)=INWRD.AND.'7
      RETURN
      END
```

Fig. C-2. Fortran IV pre-processing subroutines for low resolution radar data.

```
      SUBROUTINE DECODE (IBUF,DAYTME,ANGLE,RETURN,POWER,ILENTH)
C
C THIS SUBROUTINE DECODES THE DATA FROM THE LOW RESOLUTION RADAR SYSTEM
C TWO RECORD LENGTHS ARE POSSIBLE
C 1140 WORD RECORDS FOR INITIAL DECODING OF DATA AND PACKING
C 855 WORD RECORDS FOR PACKED DATA
C IBUF= INTEGER ARRAY WITH ONE RECORD FROM DATA TAPE
C DAYTME= INTEGER ARRAY OF DAY-TIME WORD FOR EACH LOOK ANGLE
C ANGLE= INTEGER ARRAY OF LOOK ANGLES
C RETURN= INTEGER ARRAY OF 100 RANGE BINS PER LOOK ANGLE
C POWER= INTEGER ARRAY OF POWER LEVELS FOR EACH LOOK ANGLE
C ILENTH= INTEGER LENGTH OF IBUF
C
      INTEGER IBUF(1),DAYTME(1),ANGLE(1),RETURN(1) ,IDATA(855),CLOCK
     *(7),AZ(3),DATA(2,13),POWER(1),PWR
      IF(ILENTH.EQ.855) GO TO55
C
C PACK 3 CHARACTER WORDS INTO 4 CHARACTER WORDS
C
      I=-2
      DO 10 J=1,1140,4
      I=I+3
      CALL PACK(IBUF(J),IBUF(J+1),IBUF(J+2),IBUF(J+3),IDATA(I),IDATA(I+
     *1),IDATA(I+2))
 10   CONTINUE
C
C PUT PACKED DATA BACK INTO IBUF
C
      DO 50 I=1,855
      IBUF(I)=IDATA(I)
 50   CONTINUE
 55   CONTINUE
C
C REMOVE DATA FROM IBUF
C
      NP1=1
      J=-14
 150  J=J+15
C DECODE CLOCK DATA
C
C
      CLOCK(1)=IBUF(J).SHIFT.-22
      CLOCK(2)=(IBUF(J).SHIFT.-16).AND.'17
      CLOCK(3)=(IBUF(J).SHIFT.-14).AND.'17
      CLOCK(4)=(IBUF(J).SHIFT.-12).AND.'3
      CLOCK(5)=(IBUF(J).SHIFT.-6).AND.'17
      CLOCK(6)=(IBUF(J).SHIFT.-5).AND.'7
      CLOCK(7)=(IBUF(J).SHIFT.-1).AND.'17
C
C DECODE AZIMUTH ANGLE
C
      AZ(1)=(IBUF(J+1).SHIFT.-21).AND.'7
      AZ(2)=(IBUF(J+1).SHIFT.-18).AND.'7
```

Fig. C-2. (Contd).

```
      AZ(3)=(IBUF(J+1).SHIFT.-15).AND.'7
C
C DECODE POWER LEVEL
C
      PWR  =(IBUF(J+1).SHIFT.-5).AND.'00000377
C SET LEADING BITS OF POWER LEVEL
      PWR=PWR .OR.'77777400
C
C DECODE VIDEO DATA
C
      DO 200 I=1,13
      JJ=J+1+I
  200 CALL SHFT(IBUF(JJ),DATA(1,I))
C
C FORM DAY-TIME INTEGER
C
      ICON=1000000
      DAYTME(NPT)=0
      DO 250 I=1,7
      DAYTME(NPT)=CLOCK(I)*ICON+DAYTME(NPT)
  250 ICON=ICON/10
C
C COMPUTE AZIMUTH ANGLE
C
      ANGLE(NPT)=64*AZ(1)+8*AZ(2)+AZ(3)
      IF(ANGLE(NPT).GE.360)ANGLE(NPT)=ANGLE(NPT)-360
C
C COMPUTE POWER LEVEL VOLTAGE
C
      POWER(NPT)= -PWR*500/256
C
C STORE VIDEO RETURN
C
      I=0
      DO 275 L=1,13
      DO 275 K=1,8
      I=I+1
      ISUB=NPT+(I-1)*57
      RETURN(ISUB )=DATA(K,L)
      IF(I.EQ.100)GO TO 290
  275 CONTINUE
  290 CONTINUE
      NPT=NPT+1
  300 IF(J.LE.940)GO TO 150
      RETURN
      END
```

Fig. C-2. (Contd).